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# Exploring Portability and Performance of OpenCL FPGA Kernels on HARPV2

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Washington University in St. Louis

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IWOCL '19

May 14, 2019



# Motivation

Moore's Law is "Dying"

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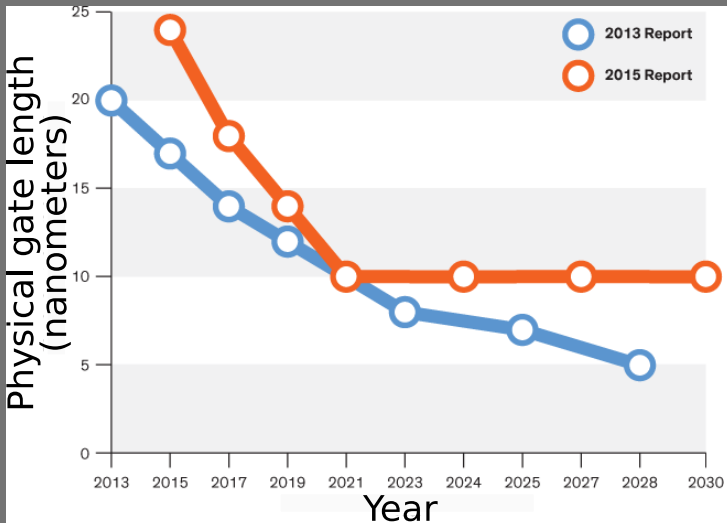
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Source:  
Courtland, IEEE Spectrum 2016



# Motivation

## Heterogeneous Systems

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Source:  
Kharya, Forbes 2018



Source:  
Forrest, TechRepublic 2017



# Motivation

## How about FPGAs?

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**Bloomberg**

Deals

## Intel's \$16.7 Billion Altera Deal Is Fueled by Data Centers

Source:  
King, Bloomberg 2015

Project Catapult

Source:  
Microsoft





# Motivation

## OpenCL to the Rescue!

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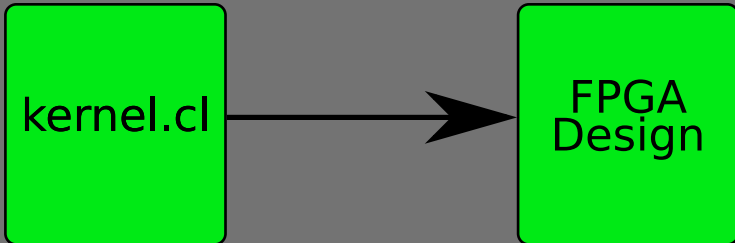
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# Motivation

## Intel's Hardware Accelerator Research Program (HARP)

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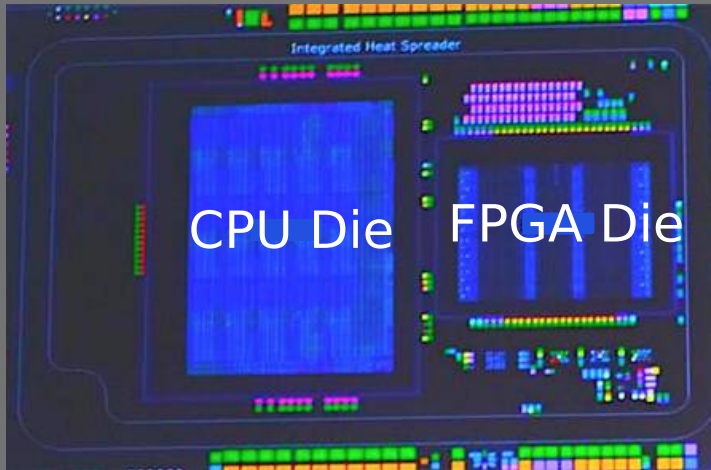
Wavefront  
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Source:

Hemsoth, The Next Platform 2016



# We address the following questions:

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- How performant and portable are OpenCL FPGA kernels on the HARPV2 platform?
- What are the hardware knobs we can turn to get the best performance?
- What is the impact of the FPGA sharing the same memory as the CPU on the HARP system?



# Outline

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# What's an FPGA, anyway?

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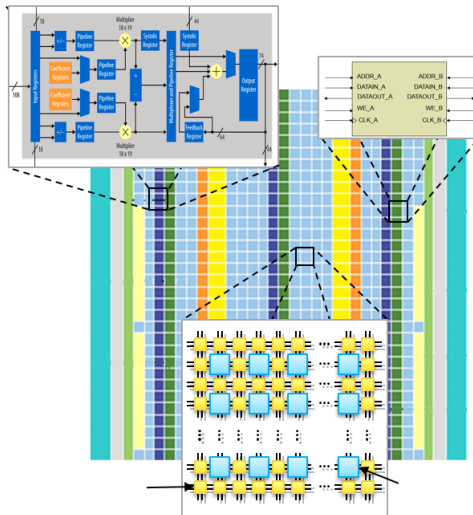
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Source:  
Intel FPGA SDK for OpenCL Pro Edition Best Practices Guide



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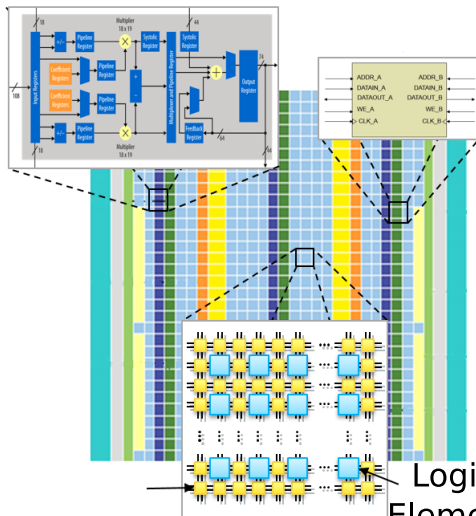
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Source:  
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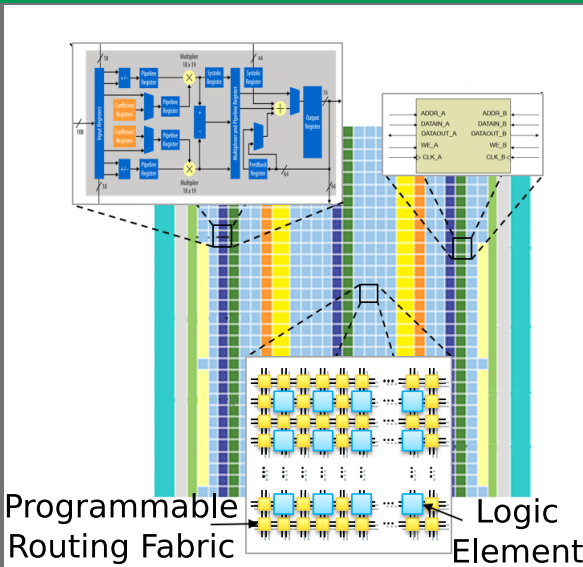
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Source:

Intel FPGA SDK for OpenCL Pro Edition Best Practices Guide



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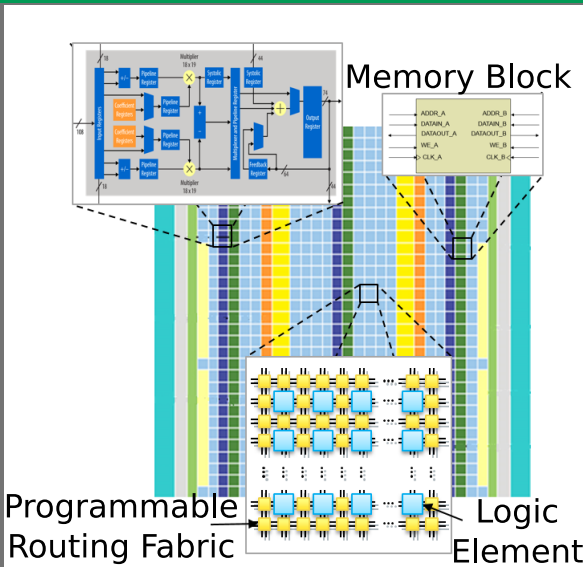
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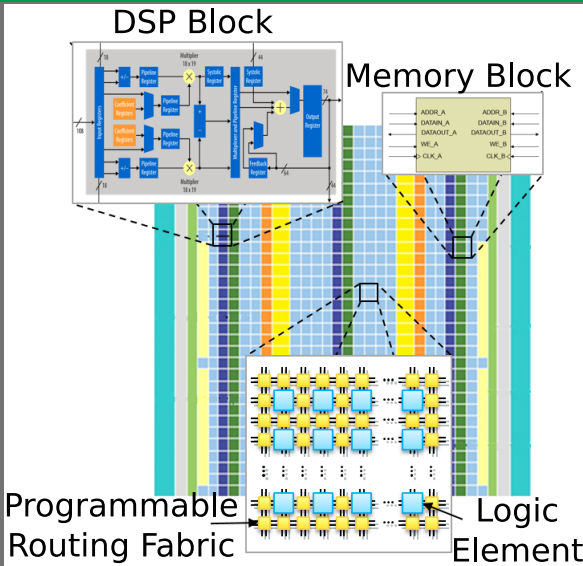
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Source:  
Intel FPGA SDK for OpenCL Pro Edition Best Practices Guide



# Discrete FPGA Card

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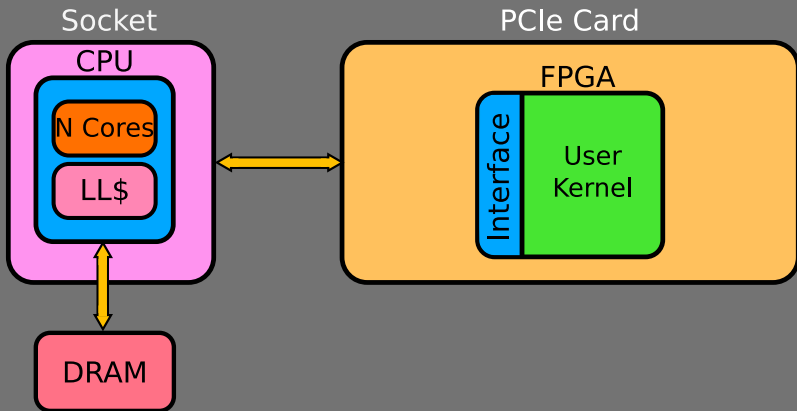
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# Intel HARPv2

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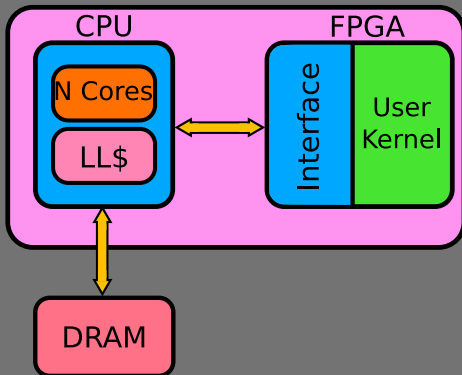
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# Intel HARPv2 (top) vs. Discrete FPGA Card (bottom)

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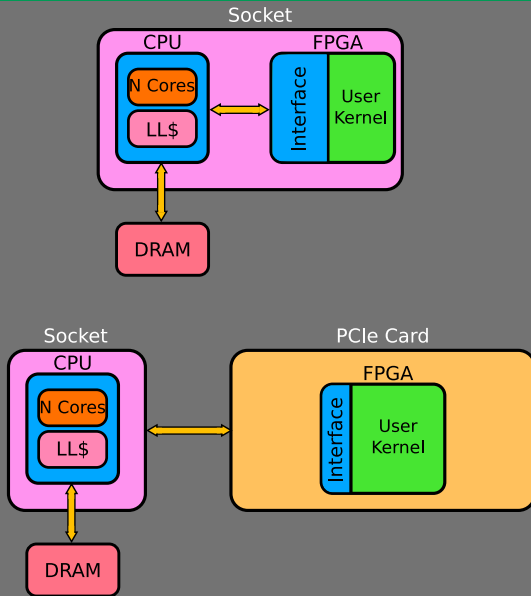
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## Dynamic Programming

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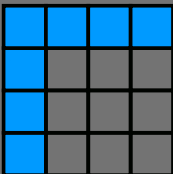
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```
1  __kernel void nw(__global int* ref_mat,  
2                      __global int* out_mat,  
3                      int  num_rows,  
4                      int  num_cols,  
5                      int  penalty)  
6  {  
7      for (int i = 1; i < num_rows; ++i)  
8          {  
9              for (int j = 1; j < num_cols; ++j)  
10                 {  
11                     out_mat[i][j] =  
12                         max( out_mat[i-1][j]      - penalty,  
13                             out_mat[i-1][j-1]    + ref_mat[i][j],  
14                             out_mat[i][j-1]      - penalty );  
15                 }  
16             }  
17         }  
18     }
```



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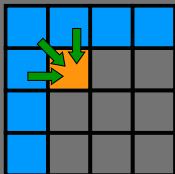
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15                 }  
16             }  
17         }  
18     }
```



# Application Flavor

$i = 1, j = 2$

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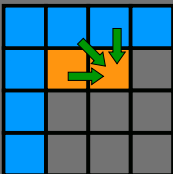
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```
1  __kernel void nw(__global int* ref_mat,
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15         }
16     }
17 }
18 }
```



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$i = 1, j = 3$

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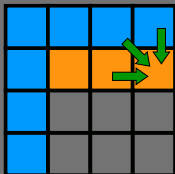
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1  __kernel void nw(__global int* ref_mat,
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15         }
16     }
17 }
18 }
```



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$i = 2, j = 1$

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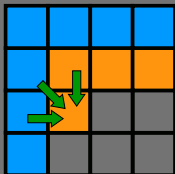
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15         }  
16     }  
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```



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$i = 2, j = 2$

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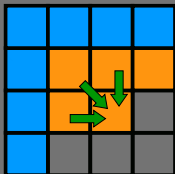
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$i = 2, j = 3$

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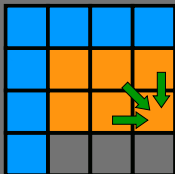
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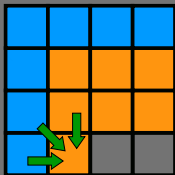
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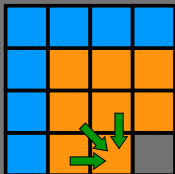
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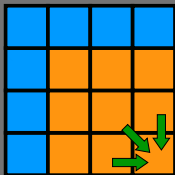
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14                     out_mat[i][j-1]      - penalty );  
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# Design Choices

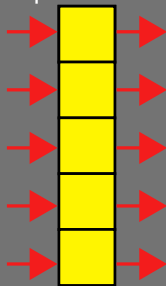
for authoring OpenCL FPGA kernels

Exploring  
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- Width vs Depth

Multiple Work Item



Single Work Item



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- Compiler Directives

---

- `reqd_work_group_size(X, Y, Z)`
- `num_simd_work_items(NUM)`
- `#pragma ivdep`  
(ignore vector dependences)
- `#pragma unroll`



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- Expressing performant FPGA constructs in High Level Language

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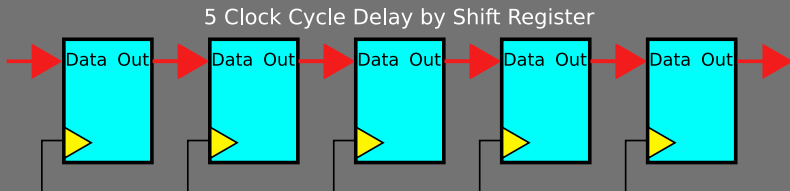
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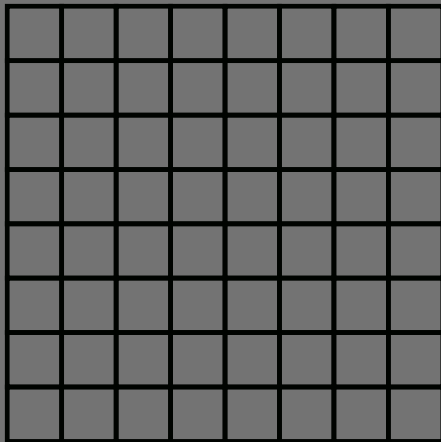
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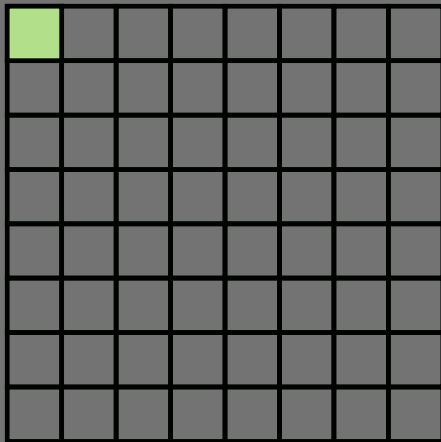
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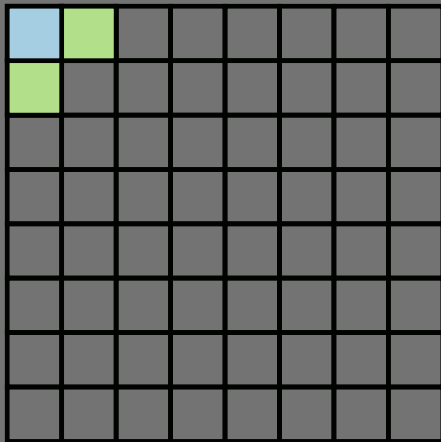
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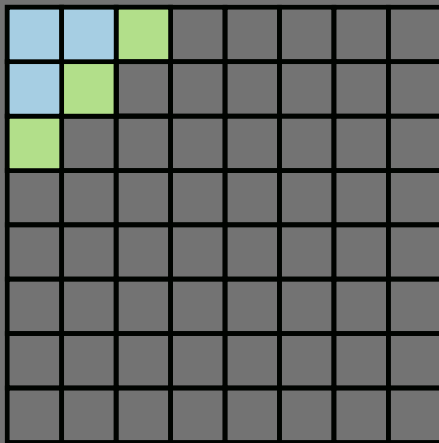
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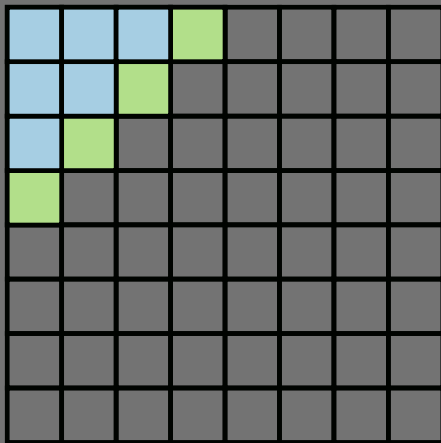
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-  Unprocessed
-  Currently Processing
-  Processed



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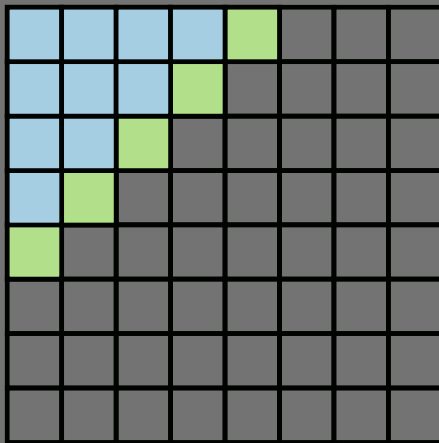
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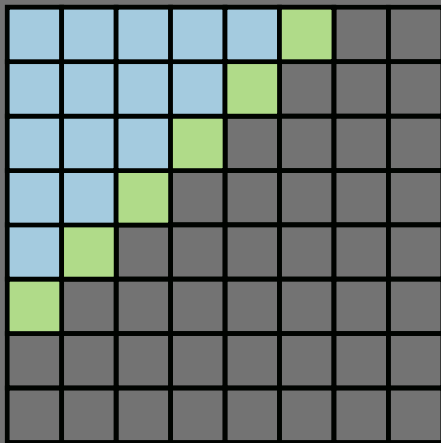
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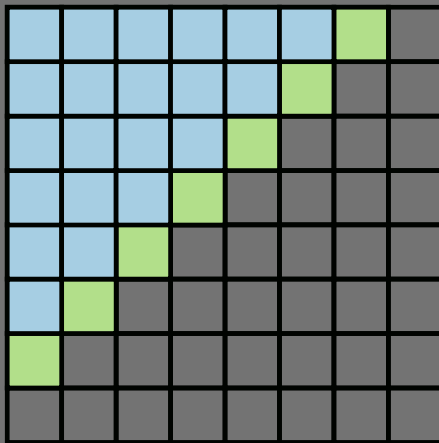
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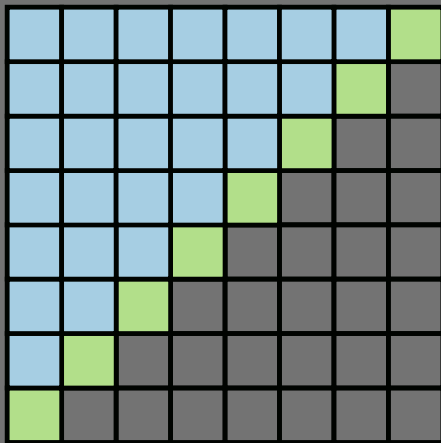
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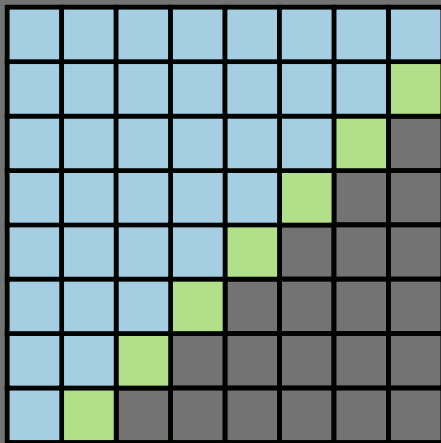
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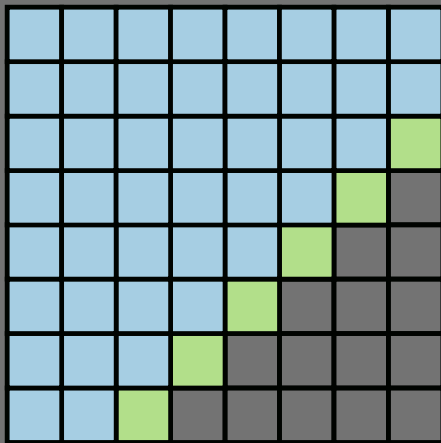
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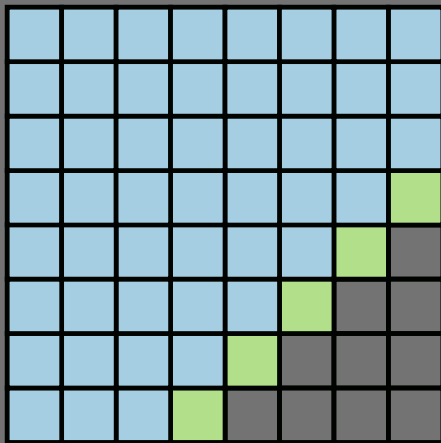
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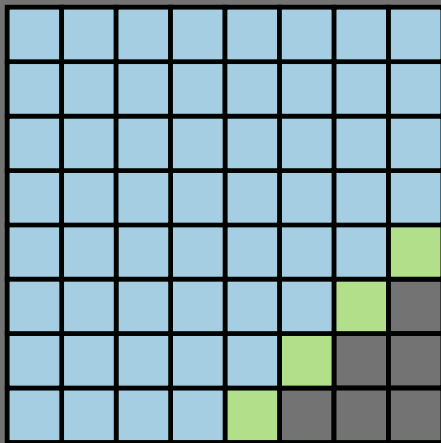
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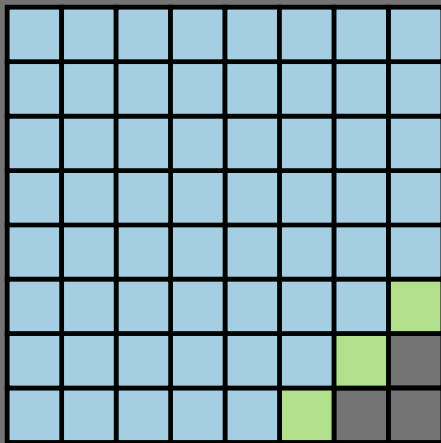
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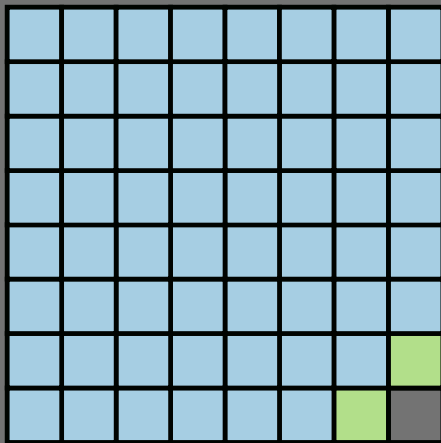
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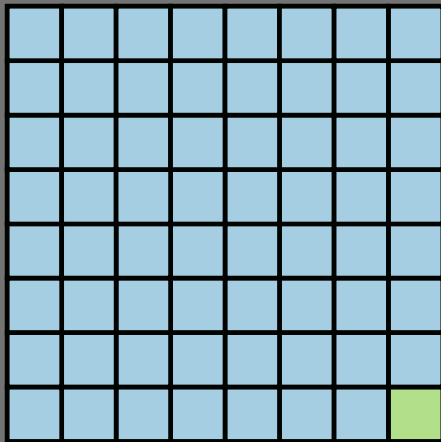
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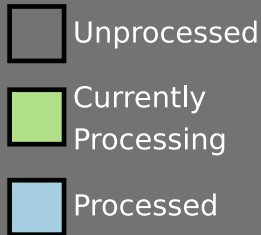
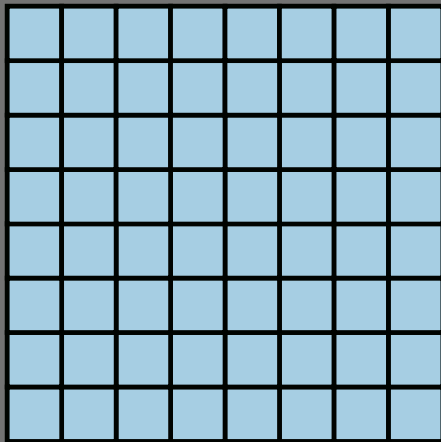
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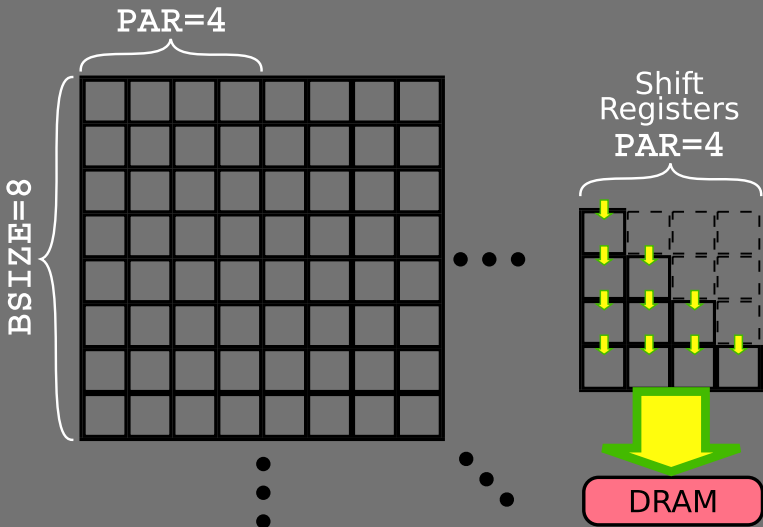
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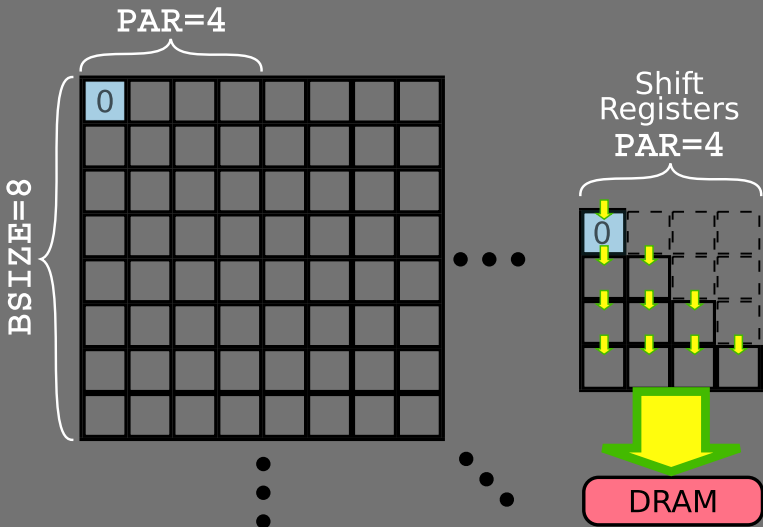
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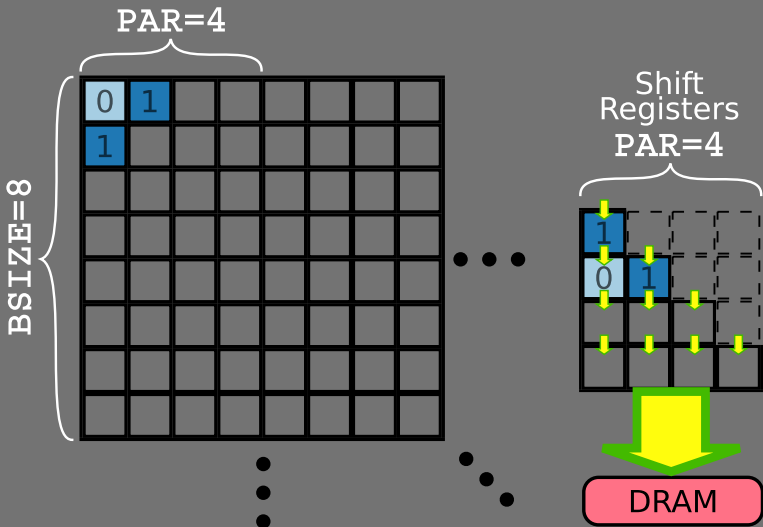
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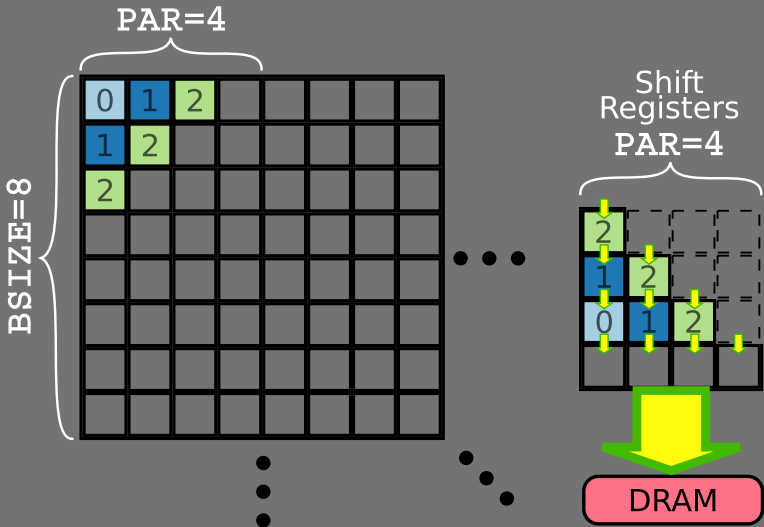
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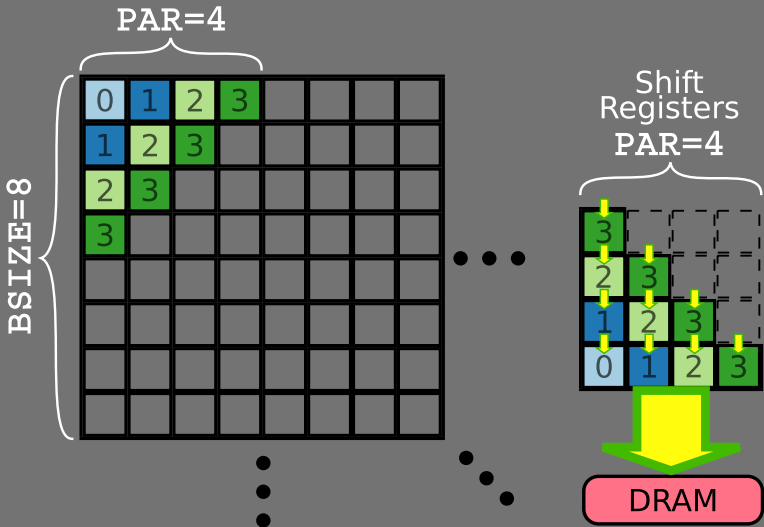
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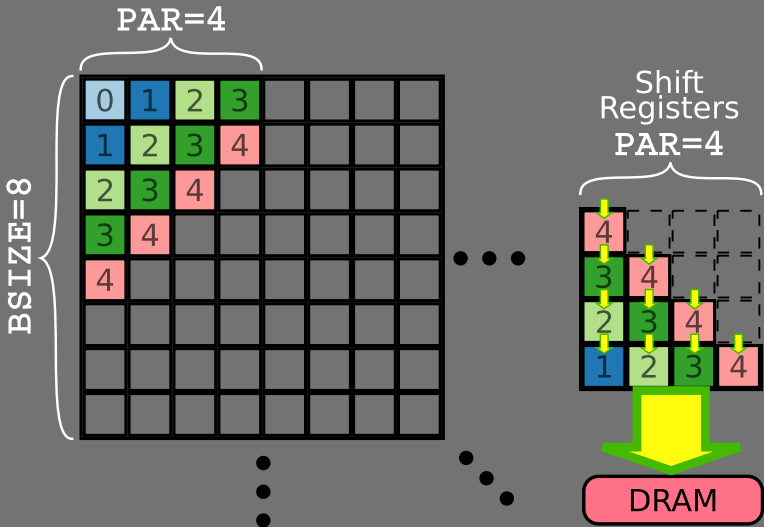
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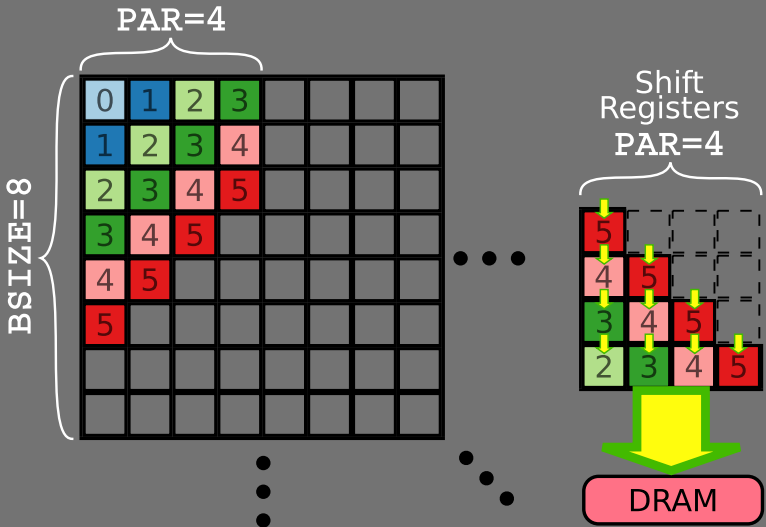
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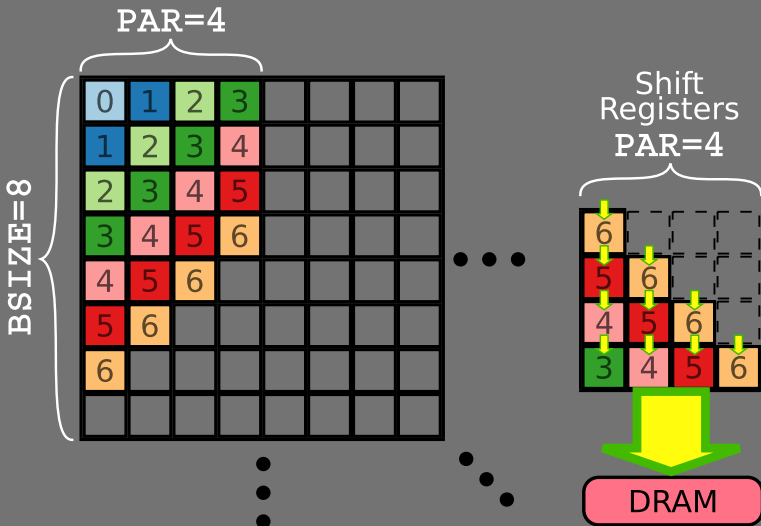
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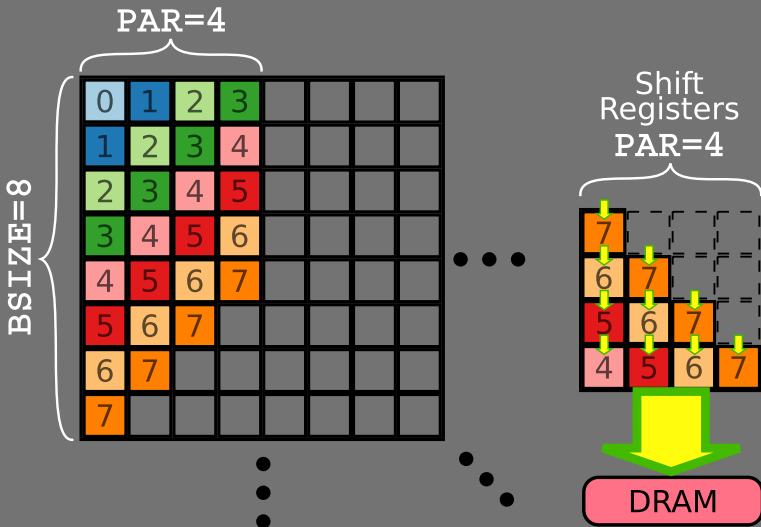
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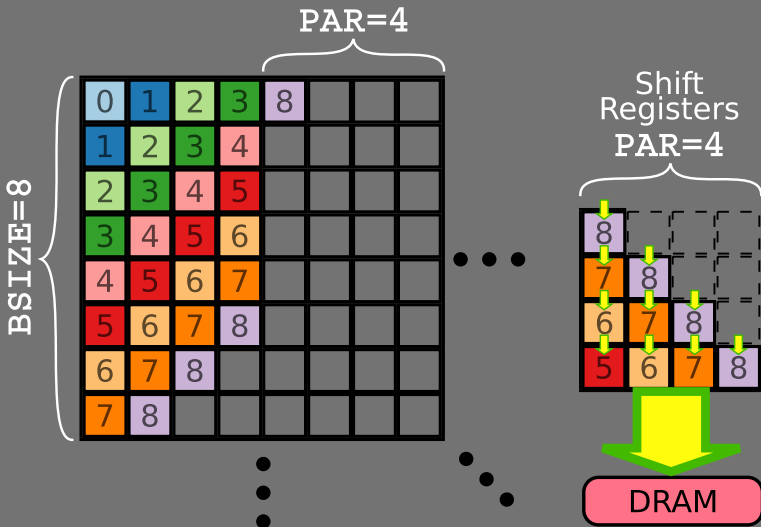
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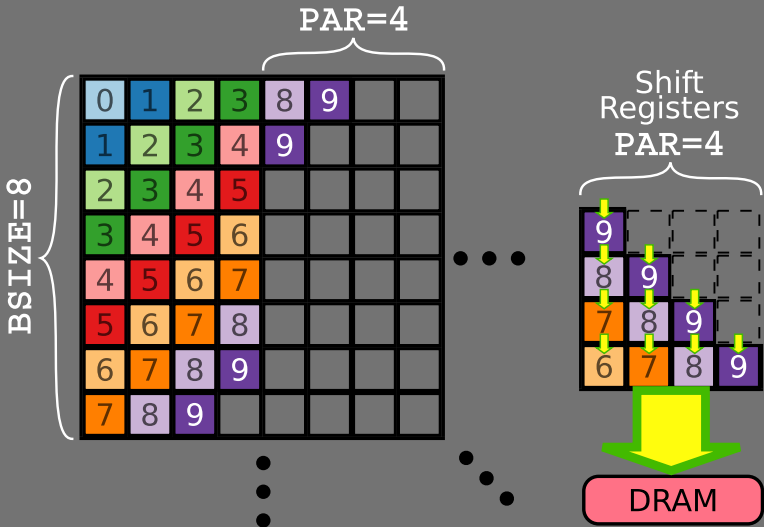
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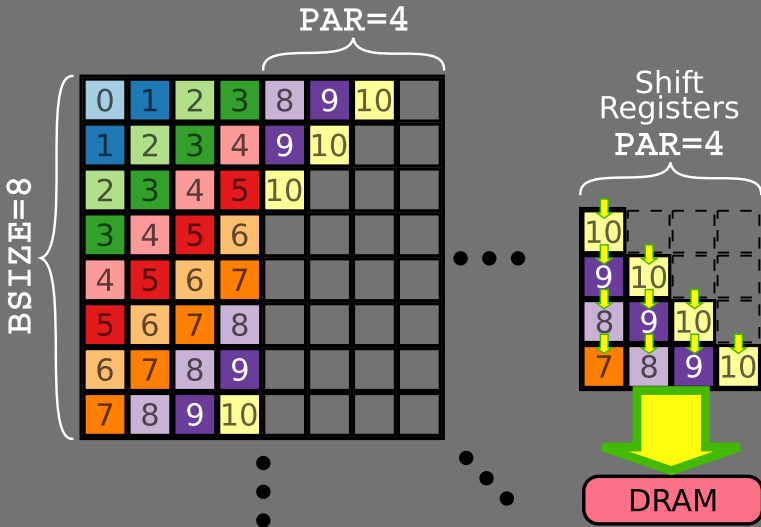
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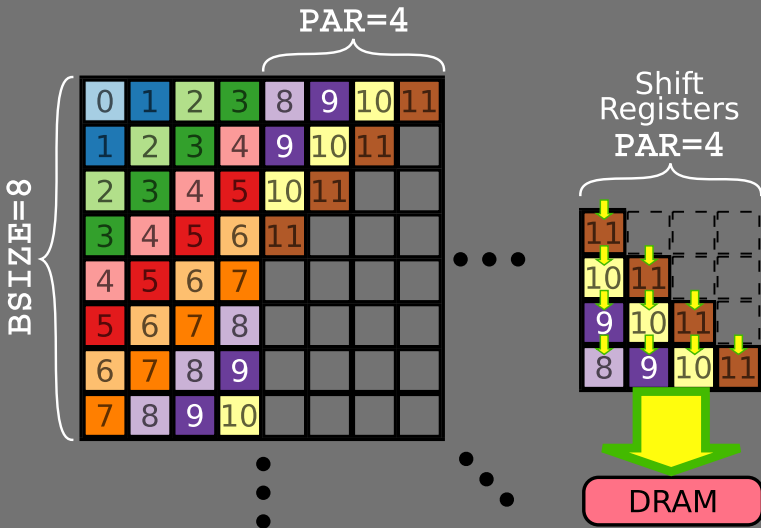
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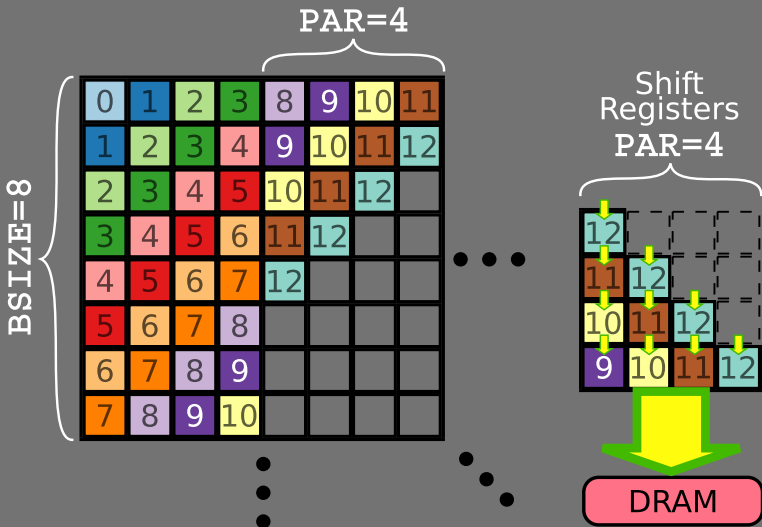
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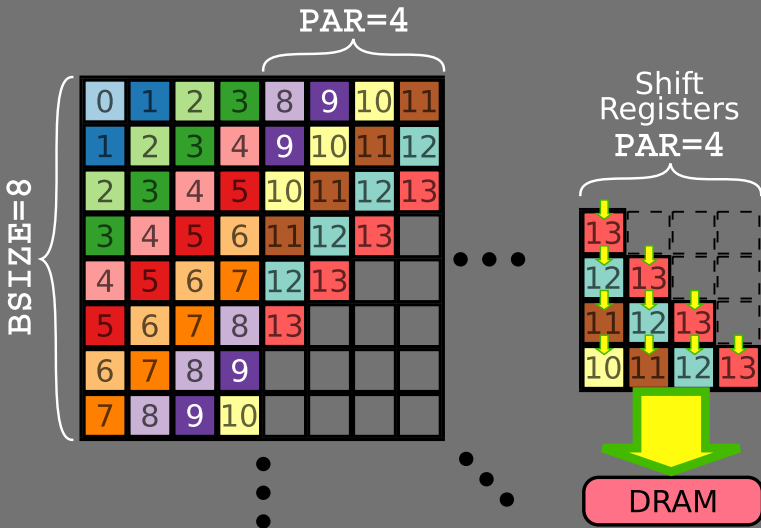
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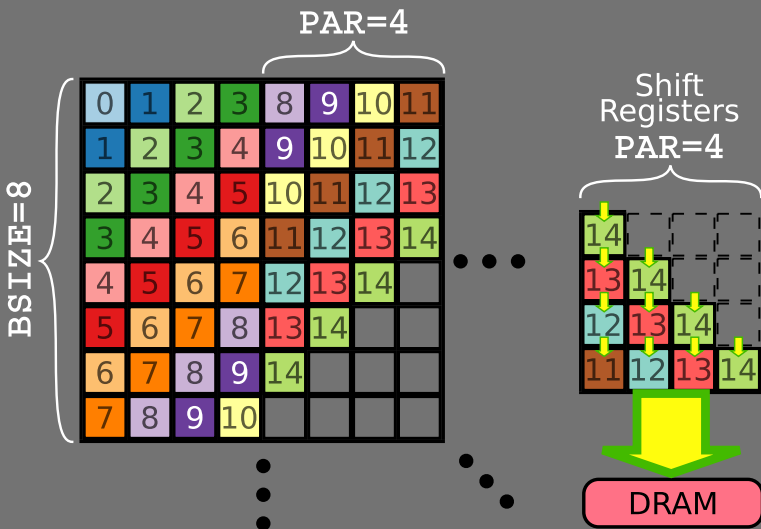
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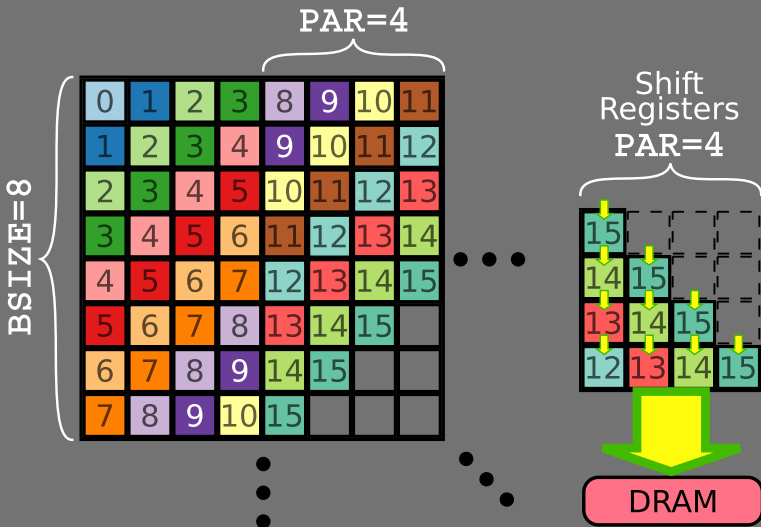
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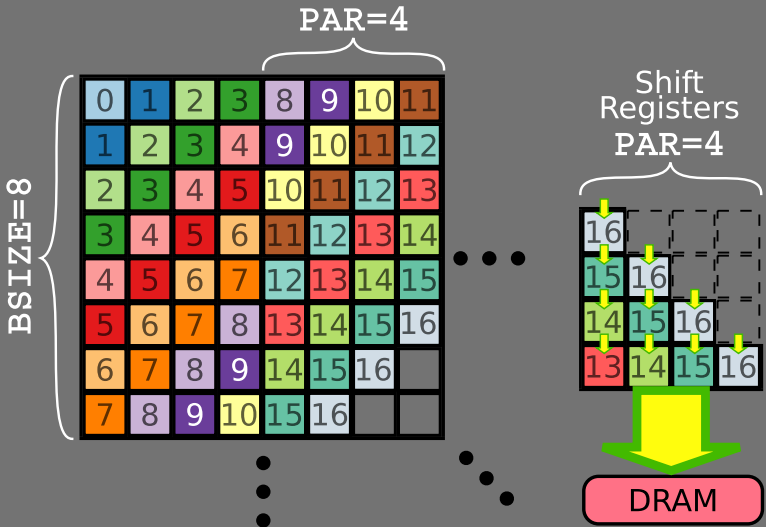
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Basic Kernel Design Choices

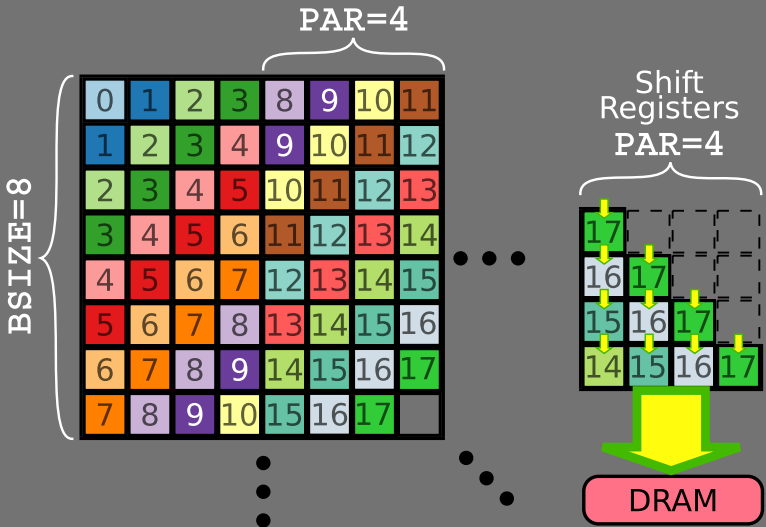
Wavefront Parallelism

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# Wavefront Parallelism

Single Work Item Blocked, Chunked

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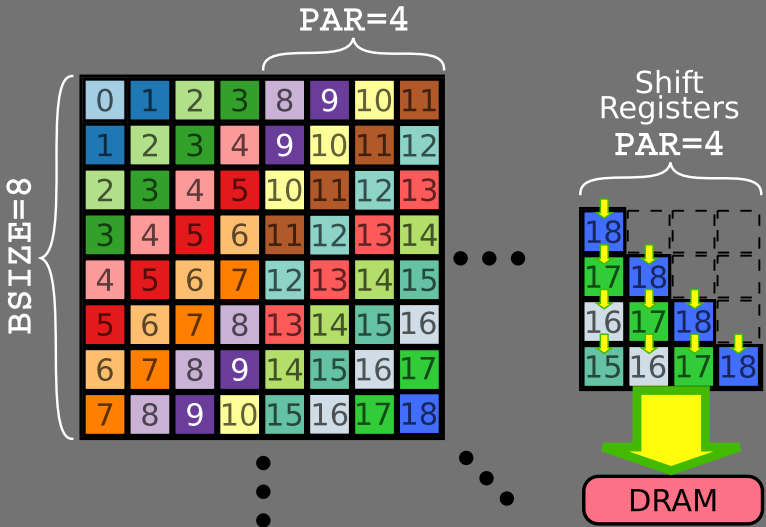
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# Hardware Design Space

Example:  $BSIZE = \{ 4, 8 \}$ ,  $PAR = \{ 2, 4 \}$

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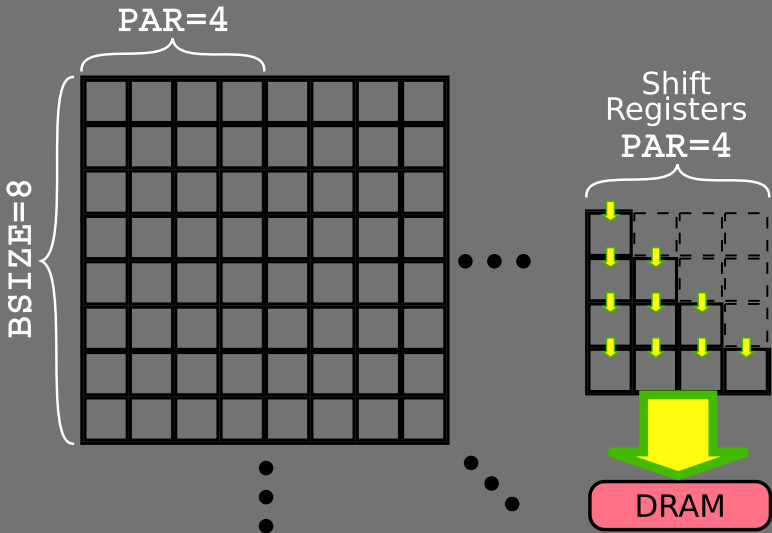
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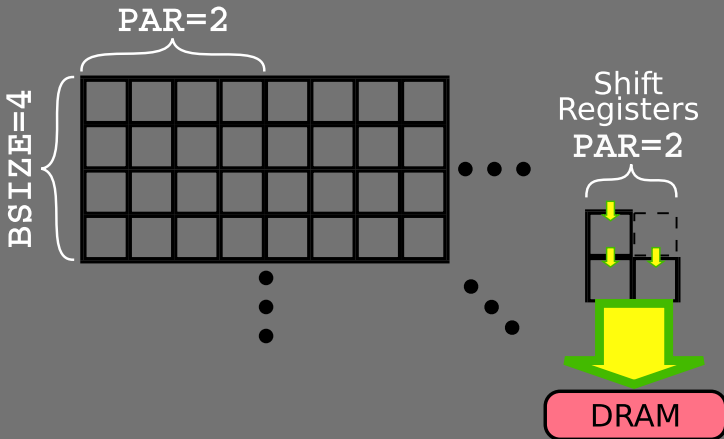
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# Shared Virtual Memory (SVM)

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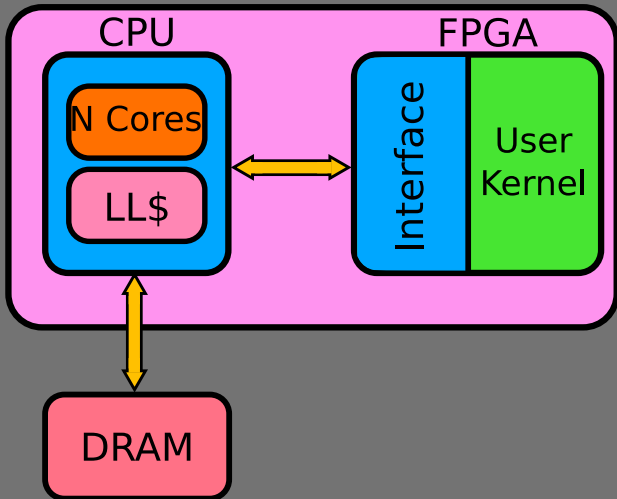
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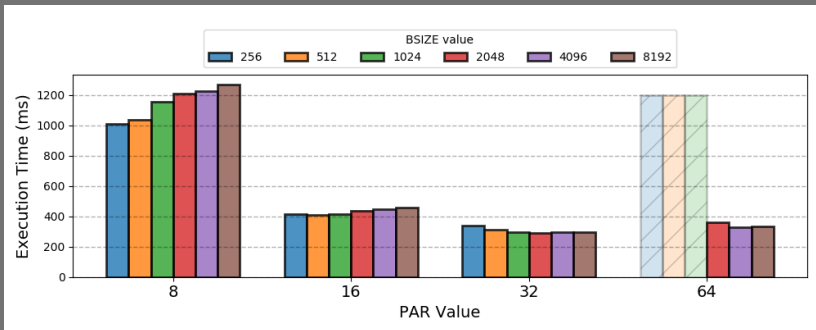
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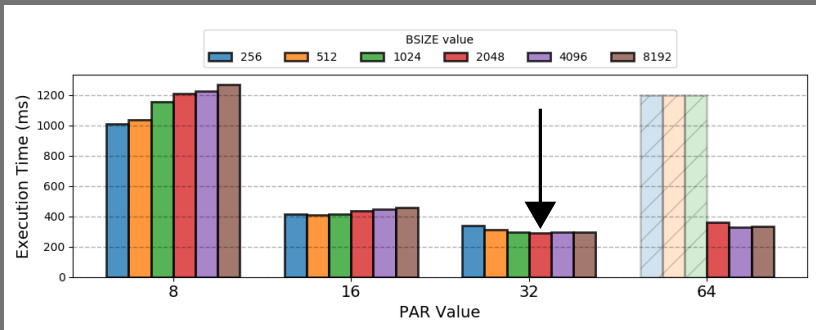
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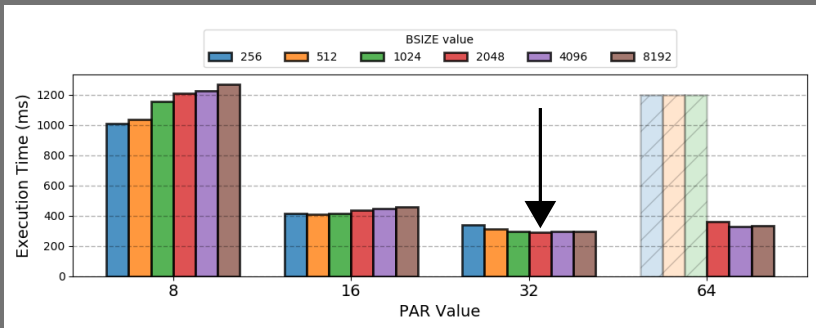
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It took 14 days to build all kernel configurations!



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- SVP = Stratix V, PCIe
- vD = Dummy
- HARP = Arria 10, HARP

V	Kernel Type	FPGA	$f_{max}$ (MHz)	Logic	Speedup
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Zohouri et al., 2018

Our Work



# Comparison Results

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v0	MWI	SVP	267.52	27%	1.00
		HARP	211.77	25%	0.74
v1	SWI	SVP	304.50	20%	0.05
		HARP	256.6	26%	0.01
v2	MWI	SVP	164.20	38%	2.48
		HARP	162.865	50%	3.90
v3	SWI	SVP	191.97	19%	3.55
		HARP	178.12	25%	3.24
v5	SWI	SVP	218.15	53%	38.22
v5	SWI	HARP	186.81	40%	34.27
vD	N/A	HARP	350.26	23%	N/A

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# Comparison Results

Exploring HARPv2

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Zohouri et al., 2018

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# SVM Results

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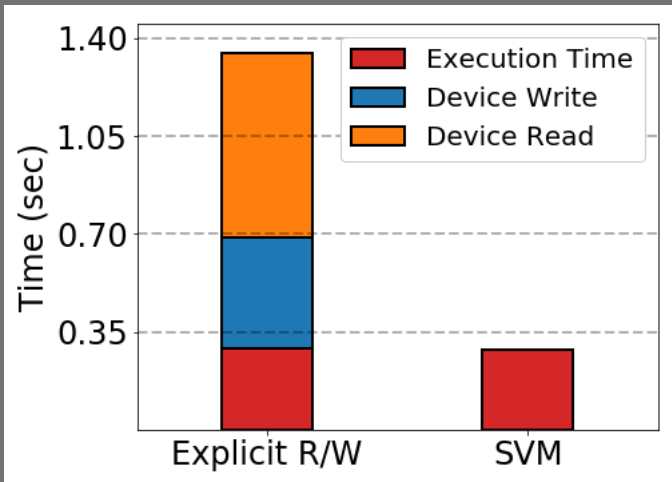
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- Design space search necessary to find most performant kernel
- OpenCL design practices for PCIe Card FPGAs hold for HARPv2
- Intel HARPv2 FPGA-CPU interface requires a lot of FPGA resources
- SVM implementation alleviates data movement problem
- For snapshot of artifacts:  
<https://openscholarship.wustl.edu/data/17/>
- For most recent updates:  
[https://github.com/cabreraam/iwocl2019\\_artifacts](https://github.com/cabreraam/iwocl2019_artifacts)