Performance Evaluation and Improvements of the *PoCL* Open-Source OpenCL Implementation on Intel CPUs

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Zuse Institute Berlin

9th International Workshop on OpenCL and SYCL, 26-29 April 2021

Motivation

- Top500 status quo: **91.8 %** of all systems feature **Intel CPUs**

TOP500 November 2020. https://top500.org/lists/top500/2020/11/

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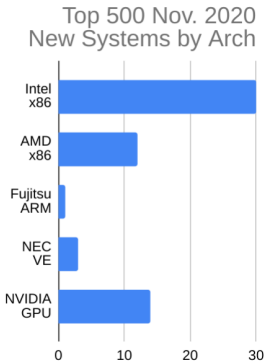
- Top500 trends: increased **diversity**
  - accelerators and co-processors (27.2 %)
  - ARM CPUs (1 %, including #1)
  - x86 CPUs from AMD (4.4 %)

⇒ **portability** more important than ever



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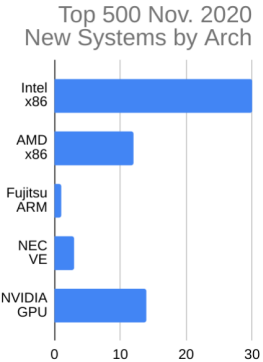
- **OpenCL** widely supported, but not every vendors 1st choice
  ⇒ vendor-independent **open source** impl.: **PoCL**



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Portable Computing Language (PoCL)

- portable, open source (MIT) OpenCL implementation
  $\Rightarrow$ maintained by Customized Parallel Computing group at Tampere University, Finland

Jääskeläinen, P., De La Lama, C. S., Schnetter, E., Raiskila, K., Takala, J., Berg, H. (2015). pocl: A Performance-Portable OpenCL Implementation. International Journal of Parallel Programming, (43)5, 752–785. https://doi.org/10.1007/s10766-014-0320-y

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  - various CPUs
  - NVIDIA GPUs via libcuda
  - HSA-supported GPUs
  - TCE ASIPs (experimental)
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- compiler: Clang/LLVM
- vectorised math libraries: SLEEF, libclc

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2. PoCL bug fixes:
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3. New PoCL CPU driver using Intel Threading Building Blocks (TBB)

4. Evaluation of vectorisation strategies and LLVM's loop and VPlan vectorisers

PoCL Work-Group Size Algorithm (simplified, for CPUs)

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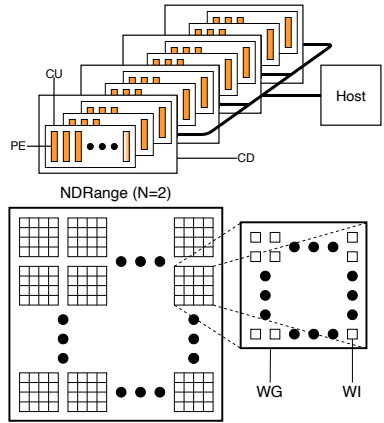

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  - maximum WG size: 4096 WI
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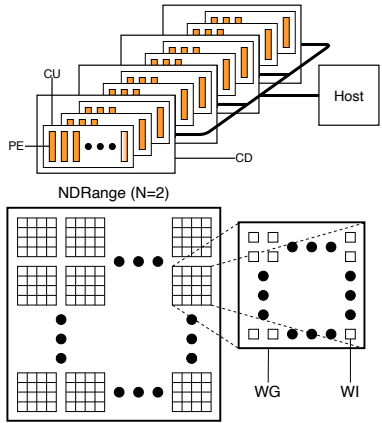

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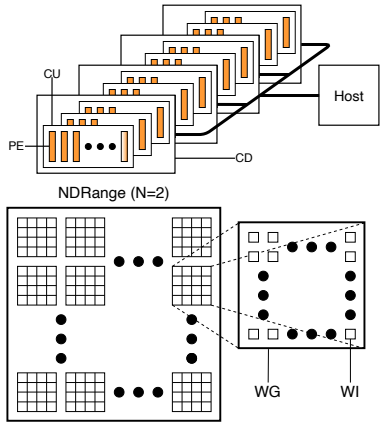
  - minimum WG size: 32 WI
  - can lead to distributions like 1.6 WGs/CU



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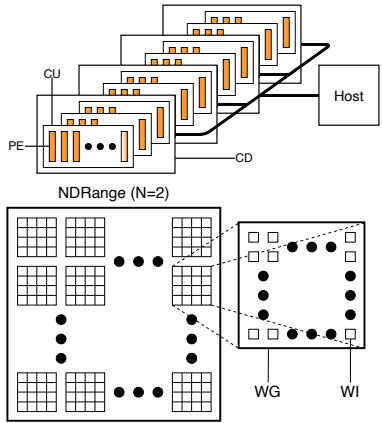

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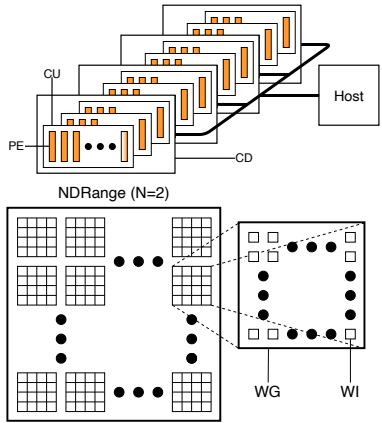

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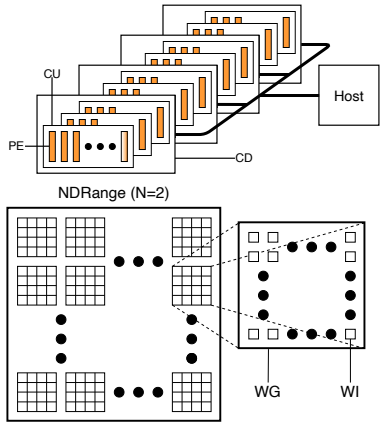

Improvement #1: minor off-by-one issue in step 2

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- example: schedule 64 WGs to 4 threads
  - balanced workload
  - no scheduling overhead

PoCL Scheduling Algorithm Balanced Workload

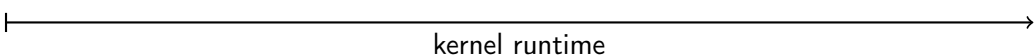
WGs remaining: 64 WGs scheduled: 0 WGs to schedule: 16

t_1:

t_2:

t_3:

t_4:



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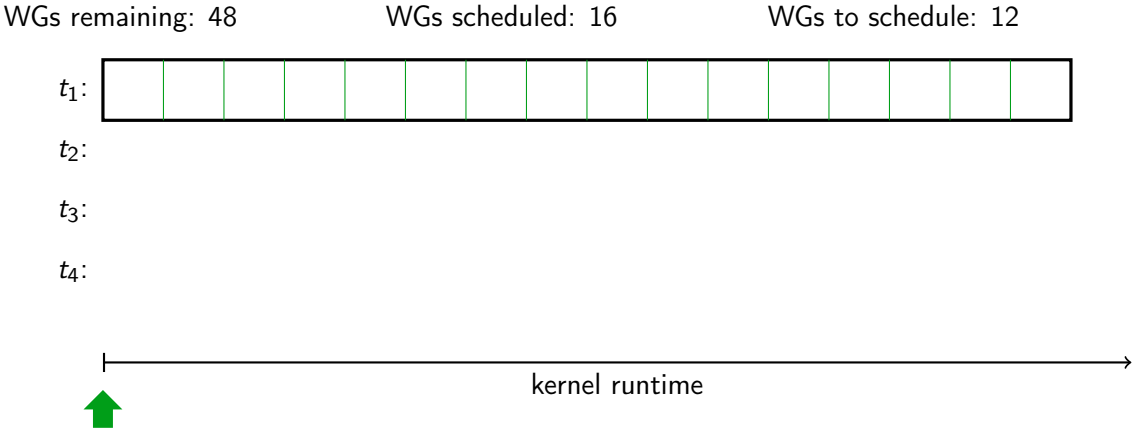

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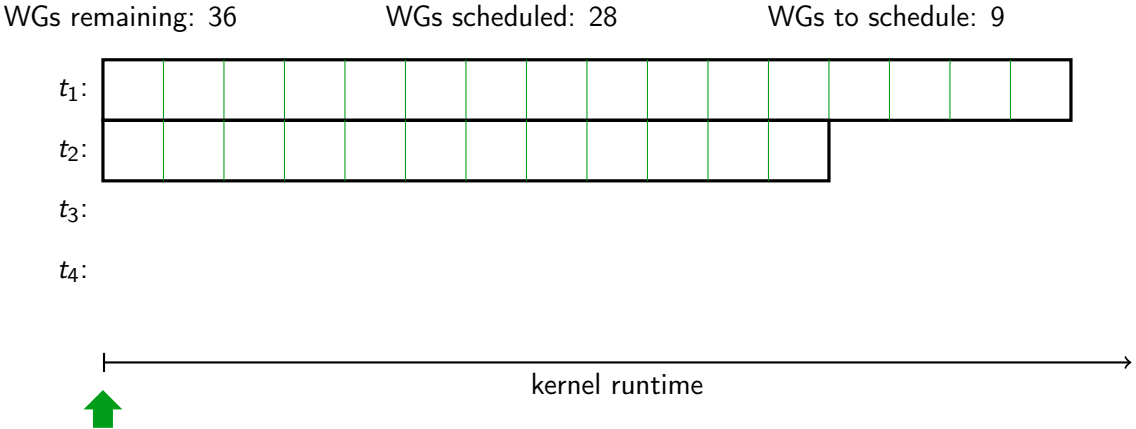

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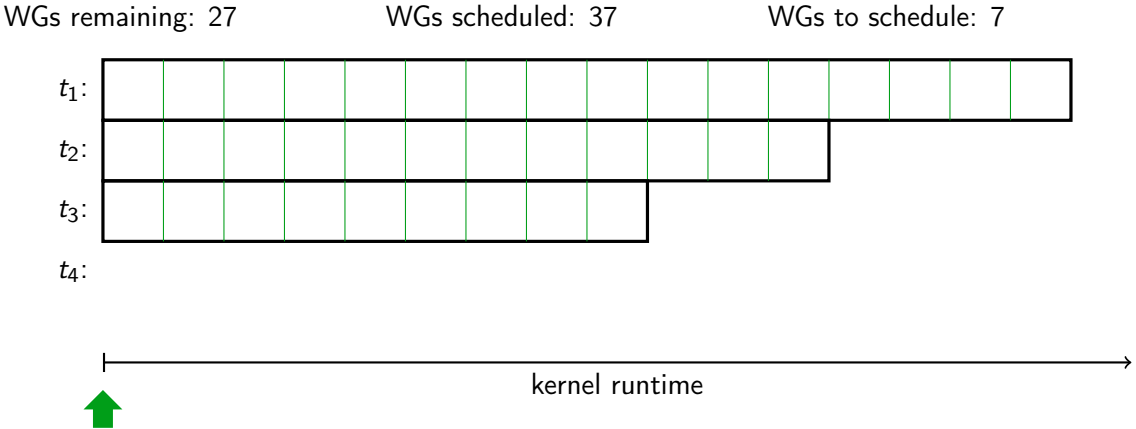
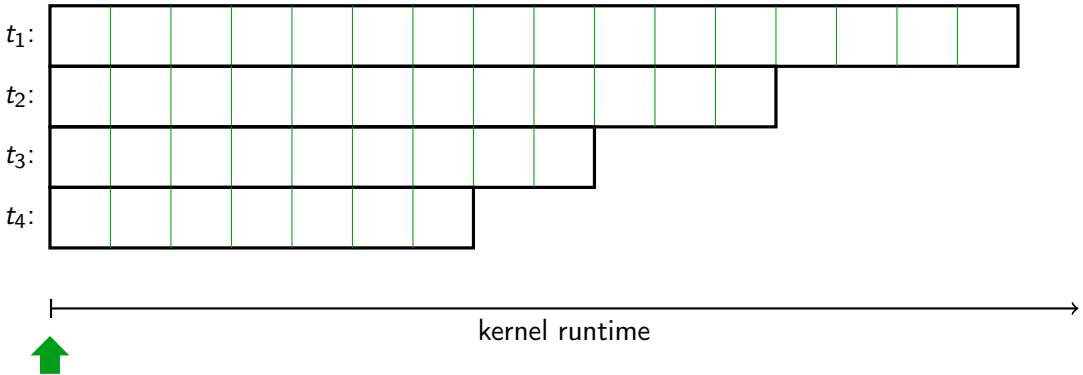


PoCL Scheduling Algorithm Balanced Workload

WGs remaining: 20 WGs scheduled: 44 WGs to schedule: 5



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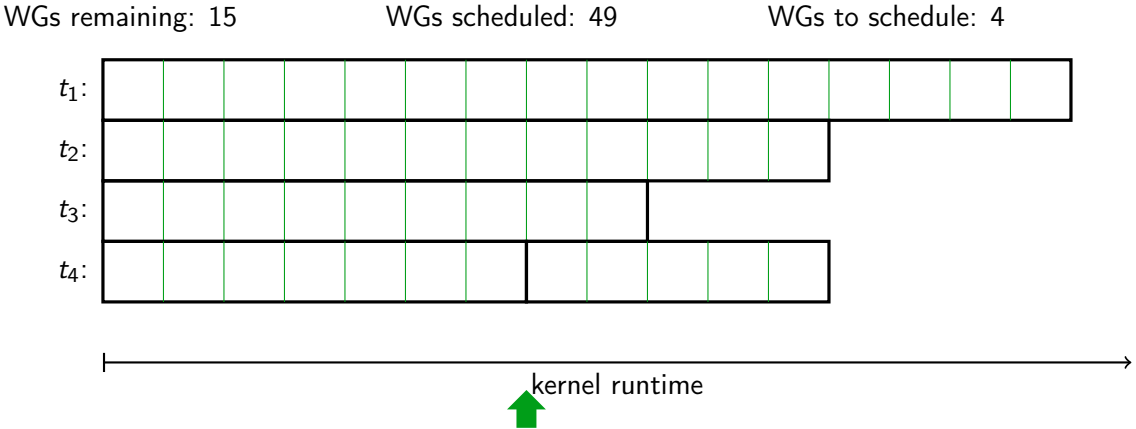
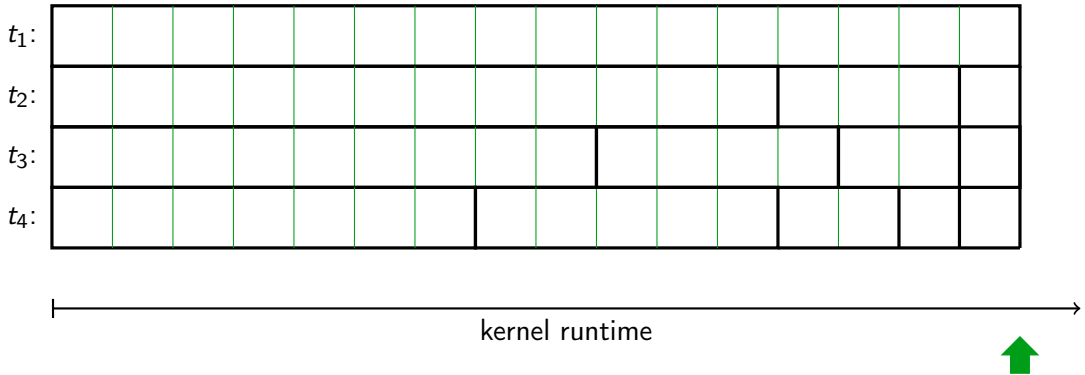


PoCL Scheduling Algorithm Balanced Workload

WGs remaining: 0 WGs scheduled: 64 WGs to schedule: -



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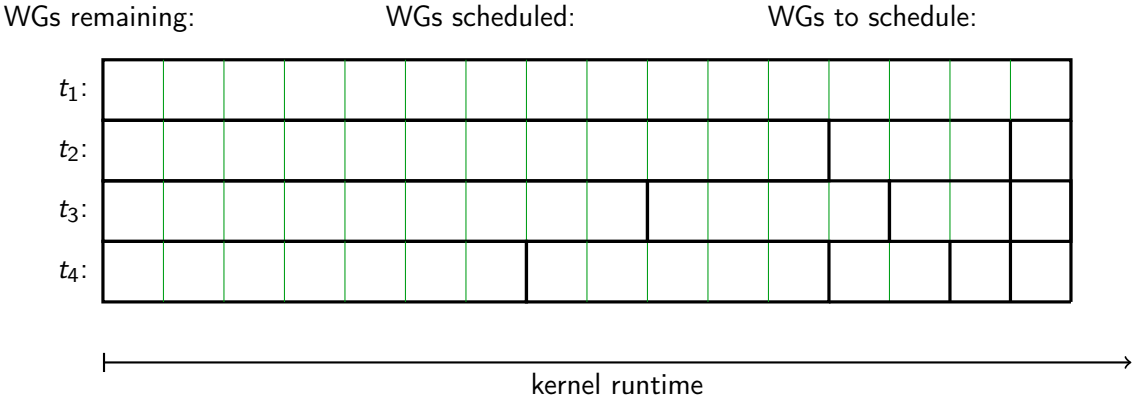
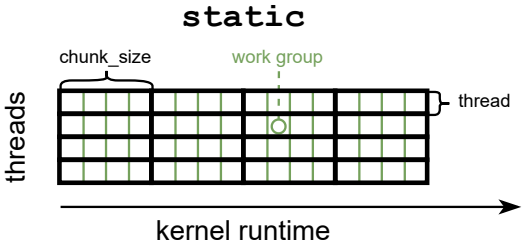


Improvement #2: integer division bug

Scheduling Algorithms: OpenMP "static" vs. PoCL "default"



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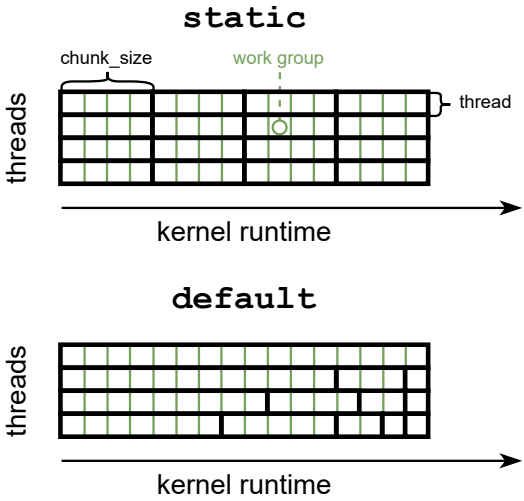

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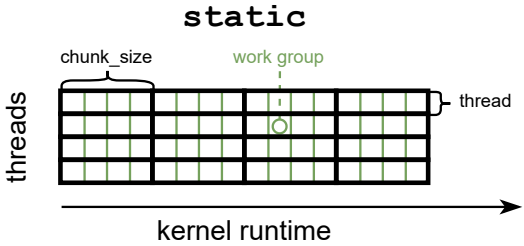

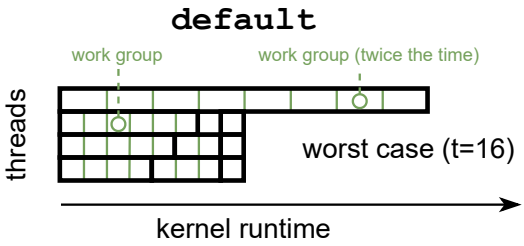

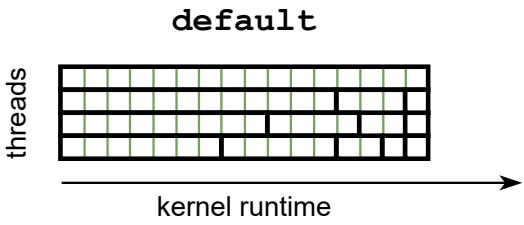

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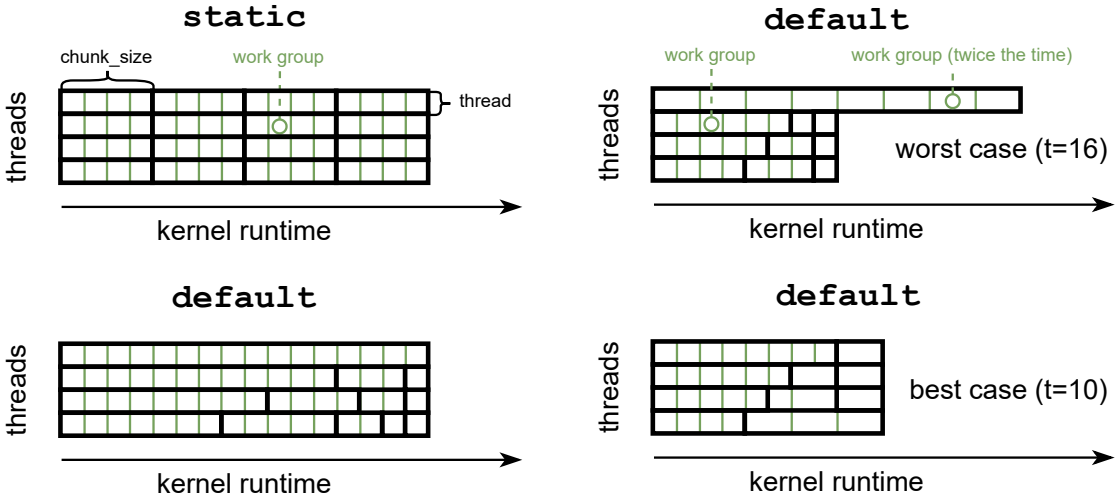

TBB device for PoCL

- Intel Threading Building Blocks (TBB) library
  - higher level alternative to *pthread*
  - used by Intel OpenCL
  - open source (Apache 2.0)
  - available **partitioners** for scheduling: auto, affinity, static, simple
  - optional parameter for all partitioners: grain size
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- Integration into PoCL:
  - derived from the *pthread* device
  - replaced relevant code sections with calls to TBB library
  - custom env vars: `POCL_TBB_PARTITIONER`, `POCL_TBB_GRAIN_SIZE`

Setup

- Software:
  - Intel CPU Runtime for OpenCL Applications 2021.1
  - PoCL 1.4 LLVM 9
  - PoCL 1.6 LLVM 11
  - PoCL 1.6 LLVM 11 with proposed TBB device

- Hardware: dual socket Intel Xeon Gold 6138 (Skylake)
  - 20 cores per socket $\Rightarrow$ 80 hardware threads
  - AVX-512 units: 2 per core $\Rightarrow$ 1 per hardware thread

Synthetic Micro Benchmark: op

- synthetic, low-level, micro benchmark
- goal: measure the performance of **operators** and OpenCL **built-in functions**

```
void op_kernel (DATA_T* in_a, DATA_T* in_b, DATA_T* out)
{
    int id = get_global_id(0);
    DATA_T tmp_a = in_a[id];
    DATA_T tmp_b = in_b[id];
    for (int i = 0; i < ITERATIONS; ++i)
    {
        tmp_a = OP_TO_BENCHMARK (tmp_a, tmp_b); //data dep.
    }
    out[id] = tmp_a;
}
```

- compile-time specialisation via: `DATA_T`, `ITERATIONS`, and `OP_TO_BENCHMARK`

Automatic vs. Manual Vectorisation

- **automatically** by the compiler or **manually** by using vector data types
- $\#WIs = \#data\_elements \div vector\_length$

- e.g. resulting ■ work-items (WIs) spanning 16 □ data elements:

vec. mode	vec. length	#WIs	logical data layout
automatic	1	16	
manual4	4	4	
manual8	8	2	

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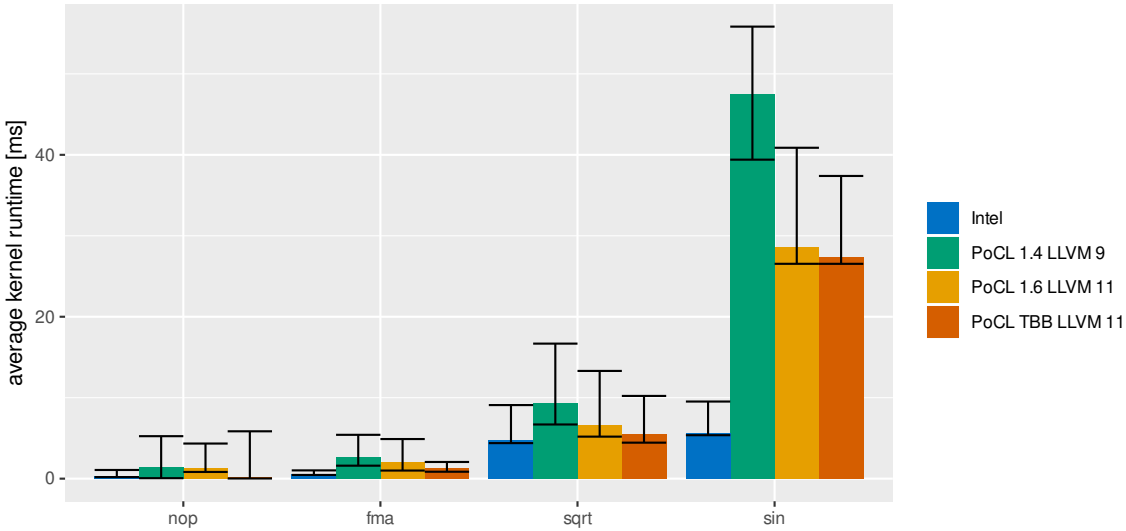

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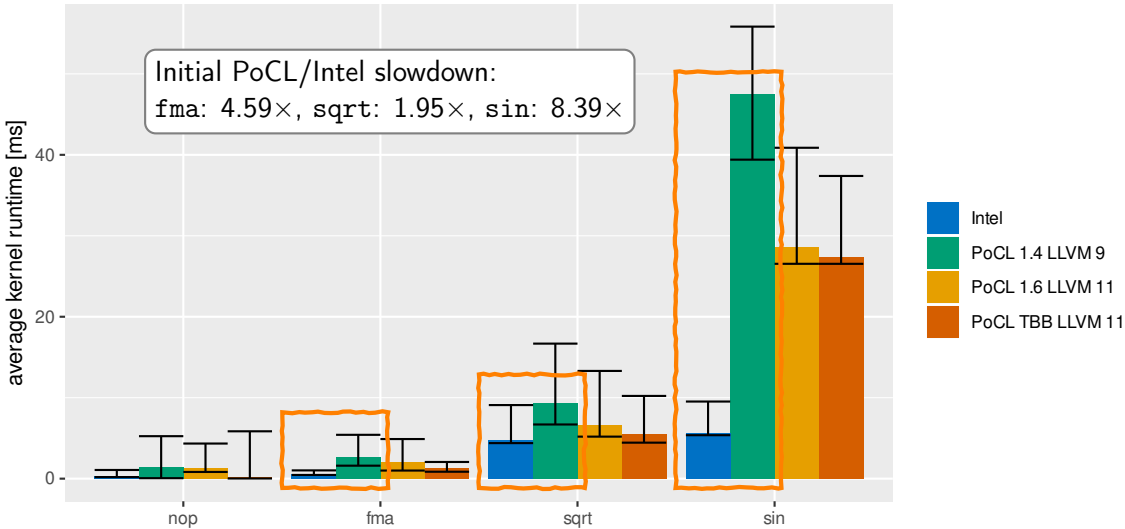

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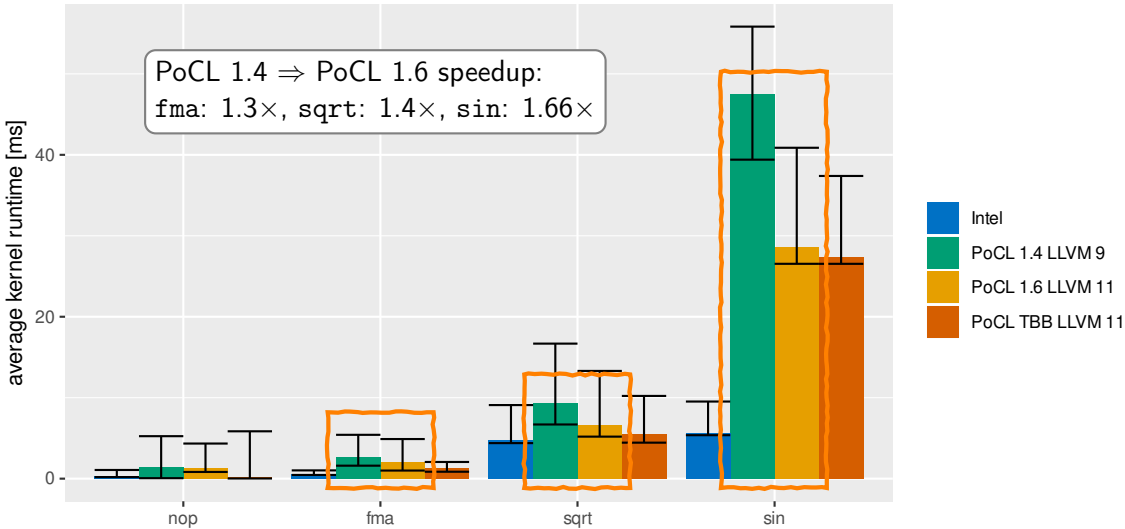

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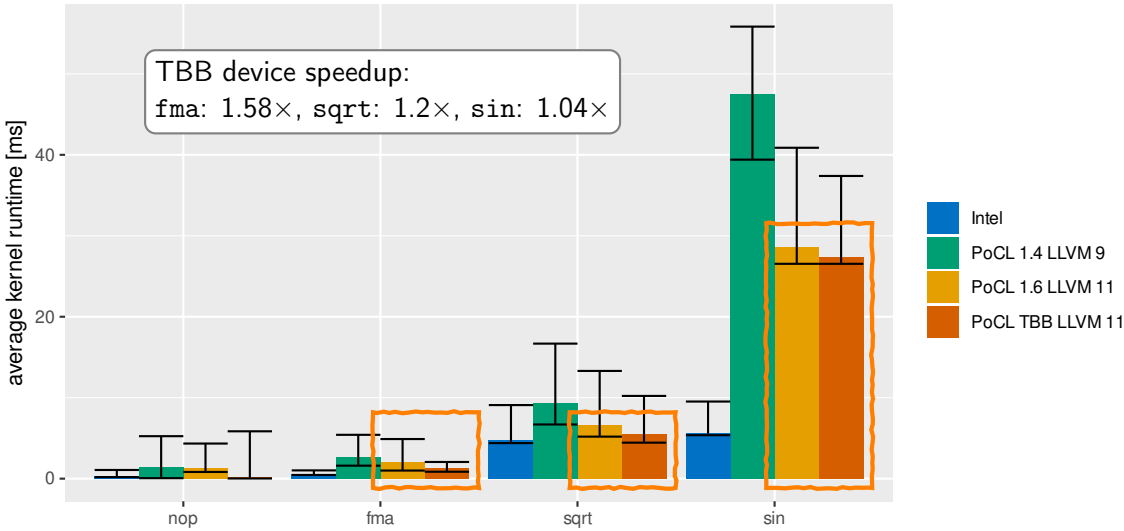

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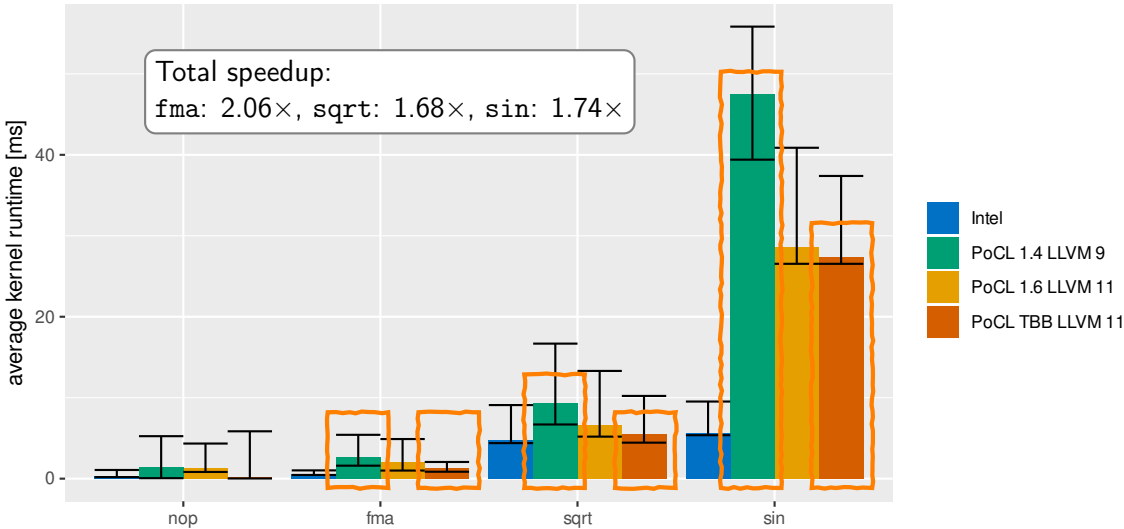
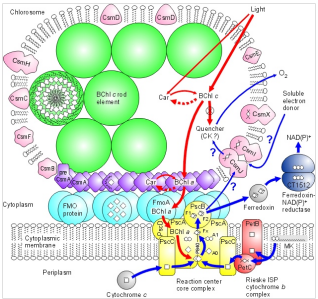


Proxy Application Benchmark: hexciton

- proxy application benchmark for the **DM-HEOM** code
- same kernel in different variants and stages of optimisation
- vectorisation strategies: **automatic** and **manual8**
- OpenMP version using KART library for runtime compilation
- instruction mix: streamlined FMA instructions
- fixed number of 512×1024 small 7×7 matrices



[Image by University of Copenhagen Biology Department]

Matthias Noack, Alexander Reinefeld, Tobias Kramer, and Thomas Steinke. 2018. DM-HEOM: A Portable and Scalable Solver-Framework for the Hierarchical Equations of Motion. In 2018 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW). 947–956. https://doi.org/10.1109/IPDPSW.2018.00149

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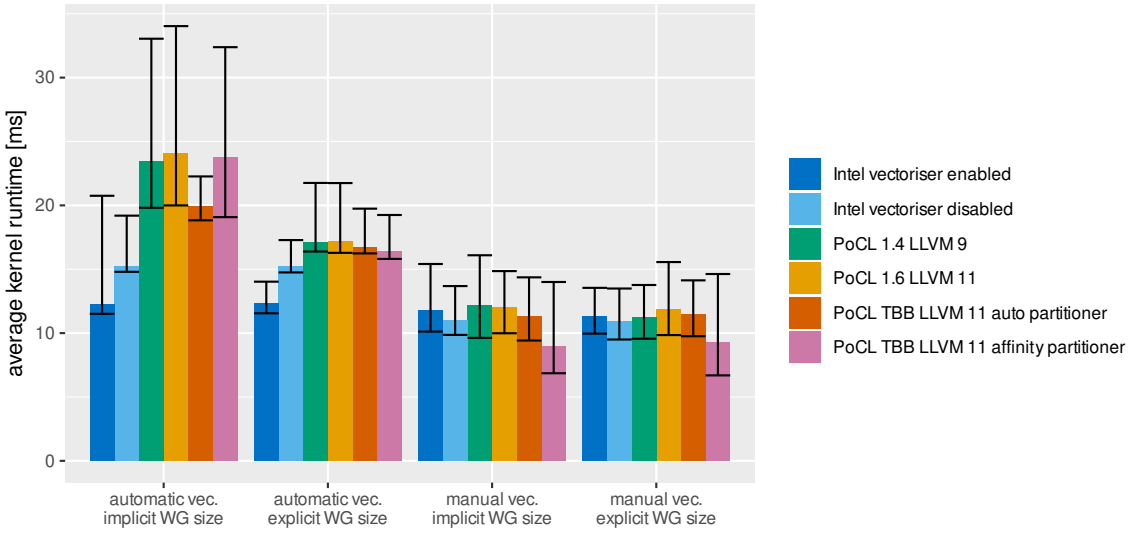

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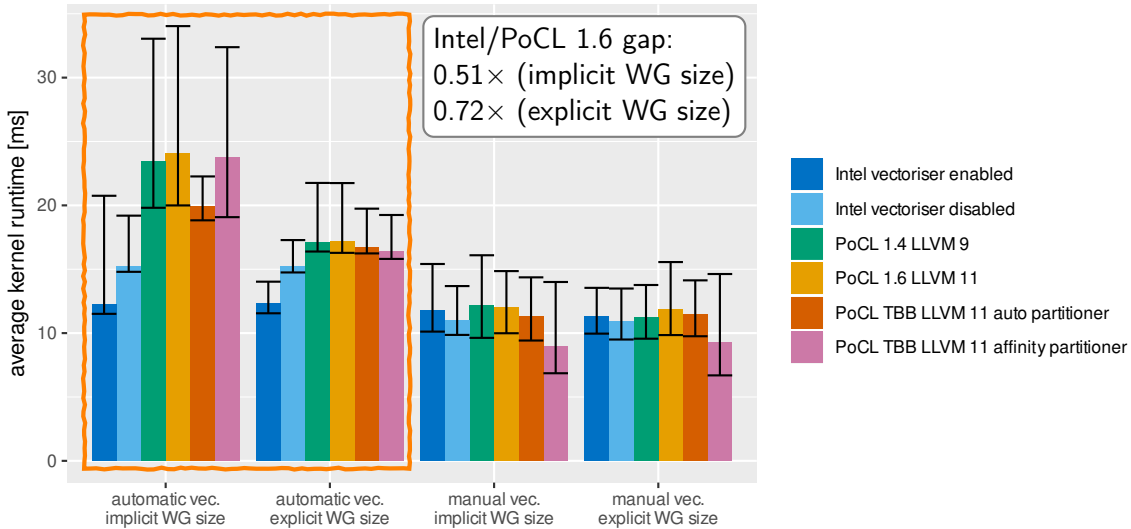

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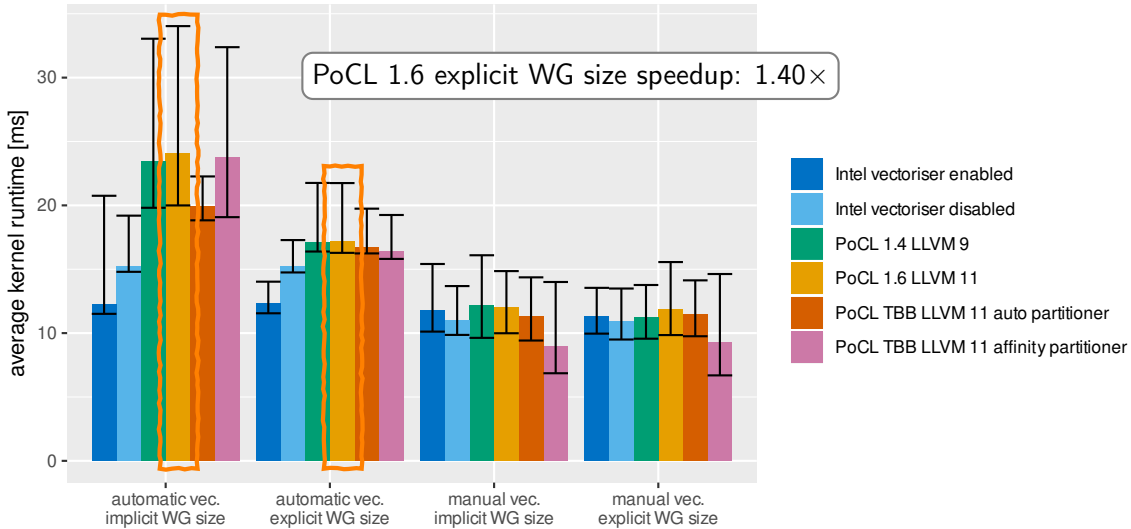

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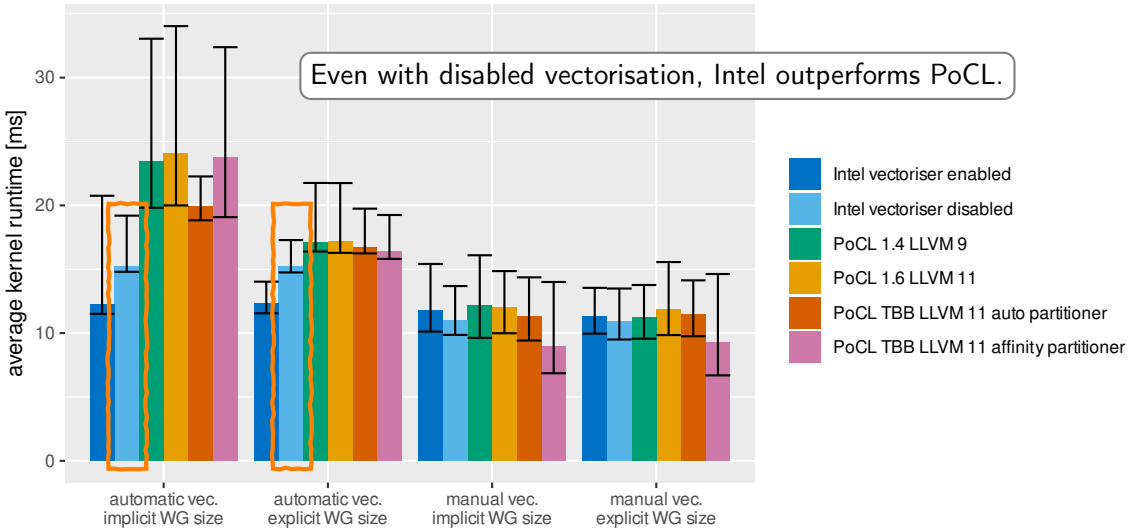

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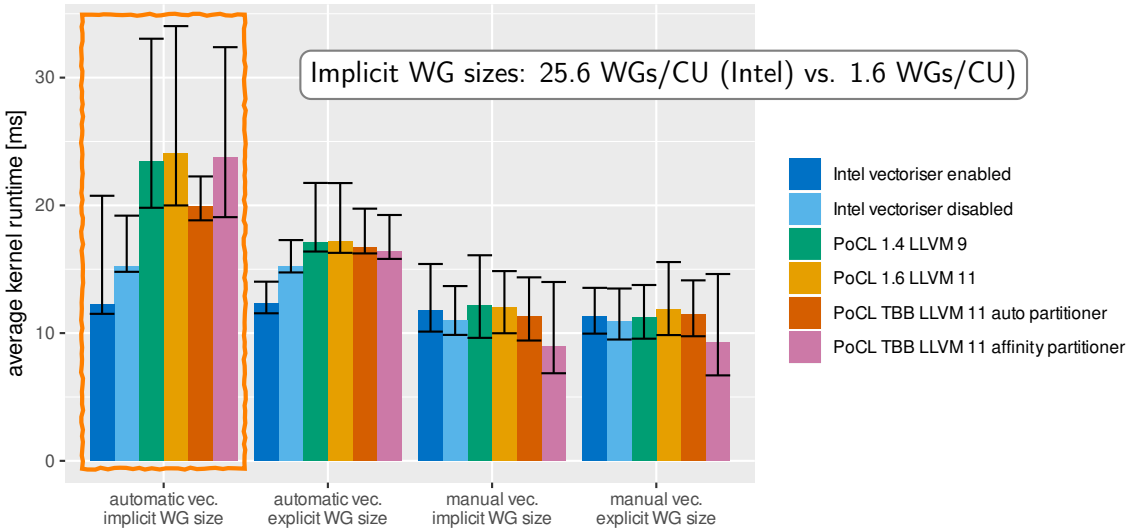

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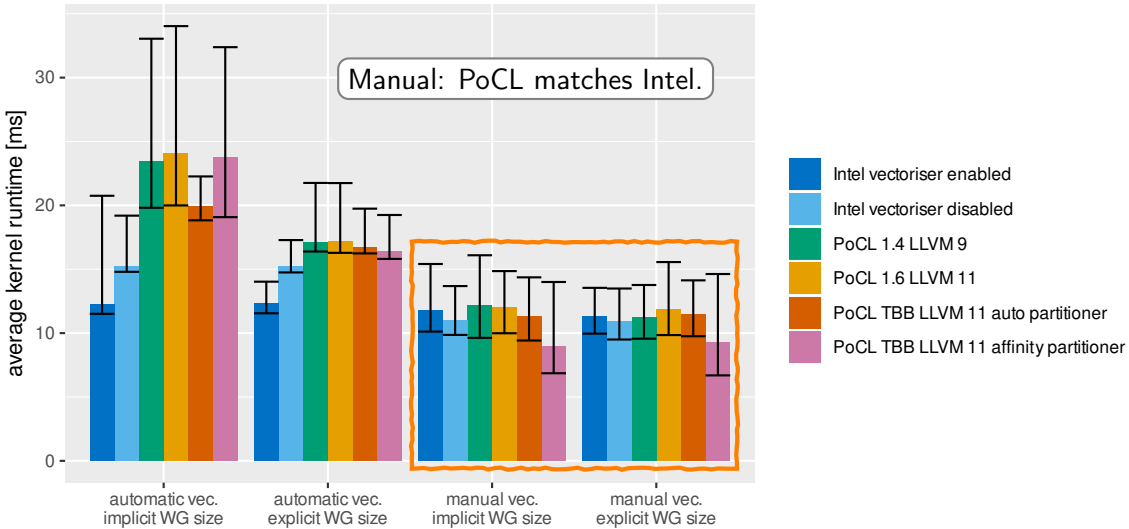

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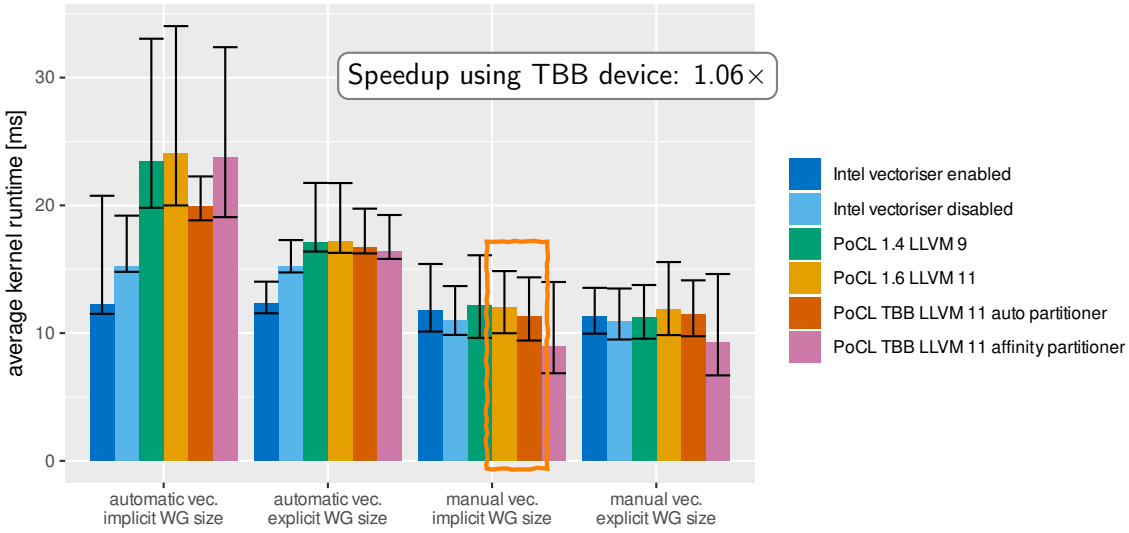

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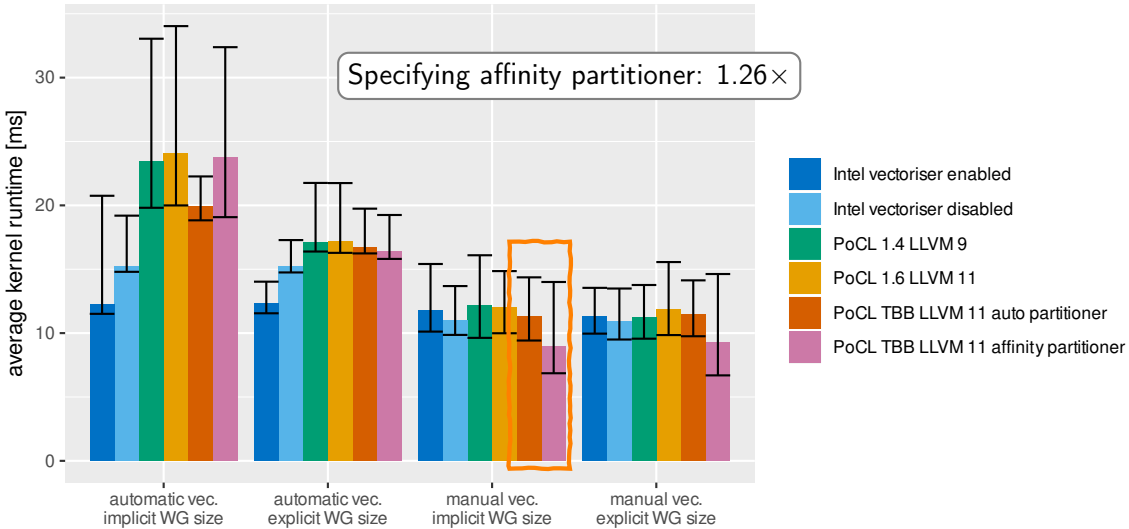

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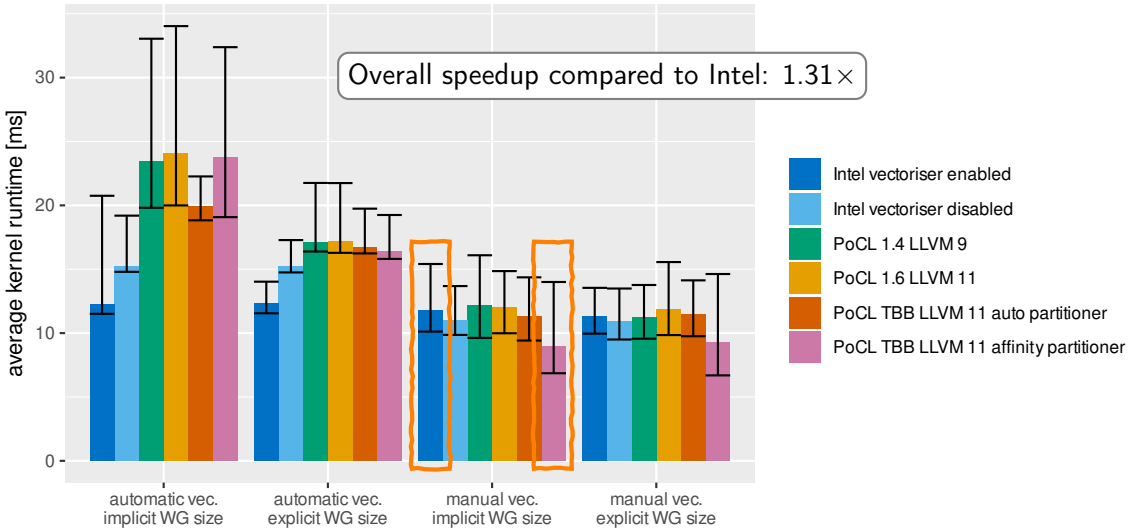
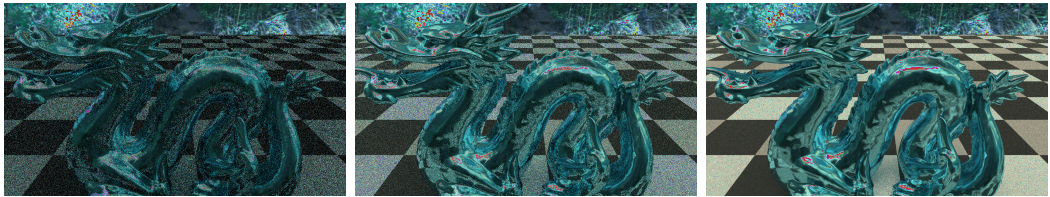


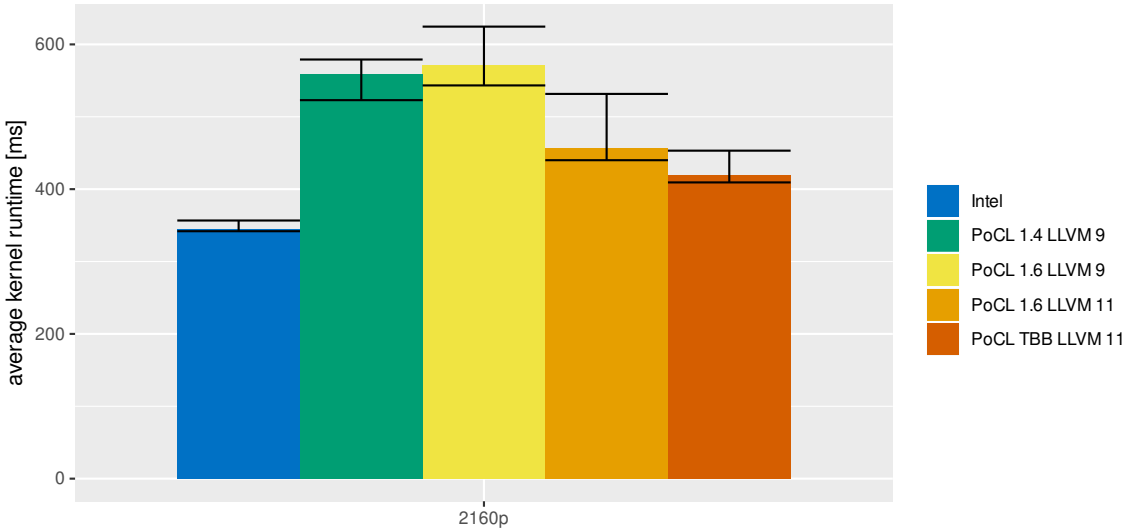
Real World Application Benchmark: raytracing

- derived from a raytracing code published on GitHub
  - $\Rightarrow$ reflect average real world application code
- more complex data structures
- work-items can take different code paths
- contains trigonometric and various other built-in functions



Raytracing benchmark source code on Github. https://github.com/new2f7/RayTracing

Real World Application Benchmark: raytracing



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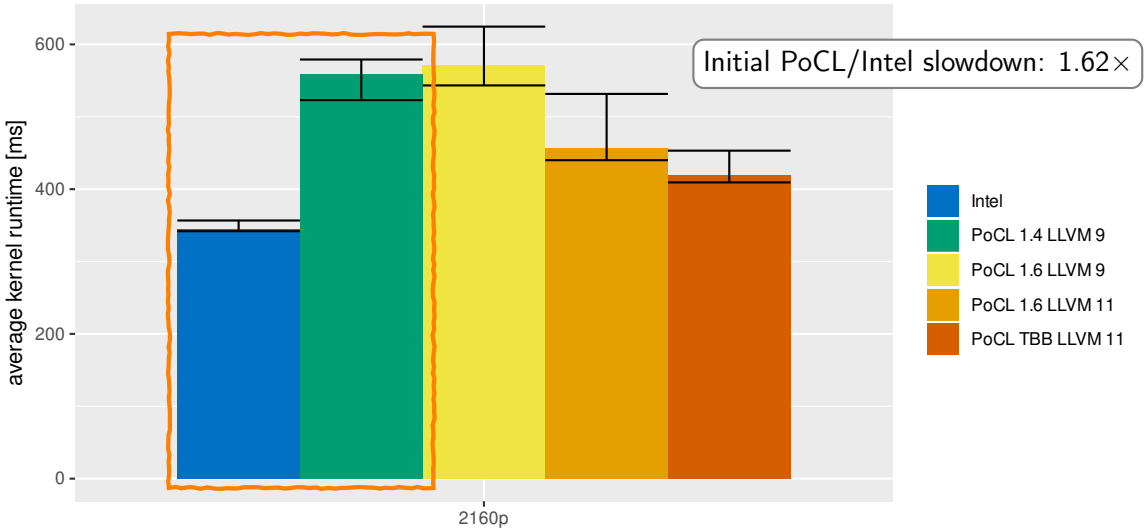

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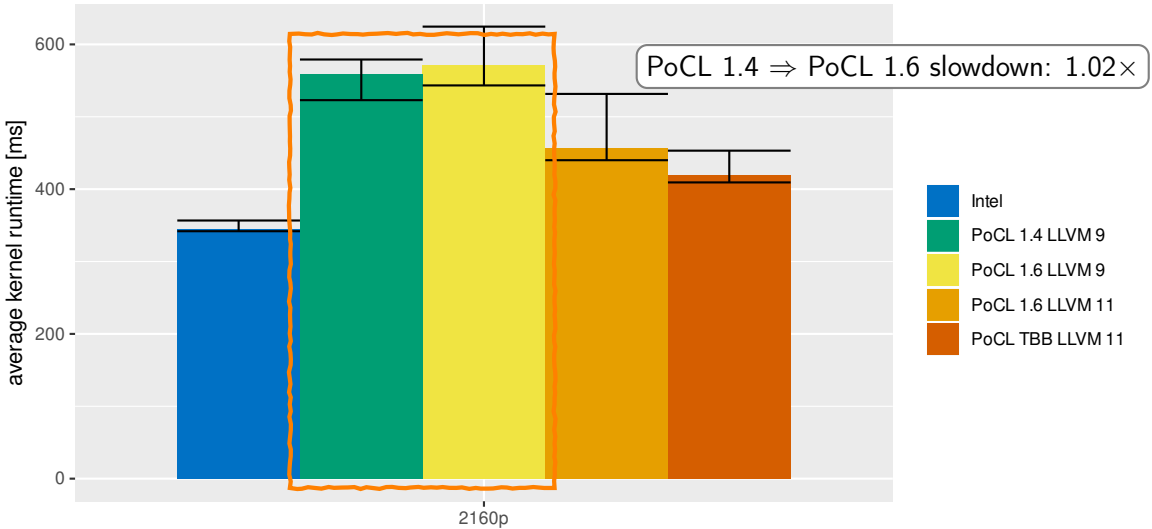

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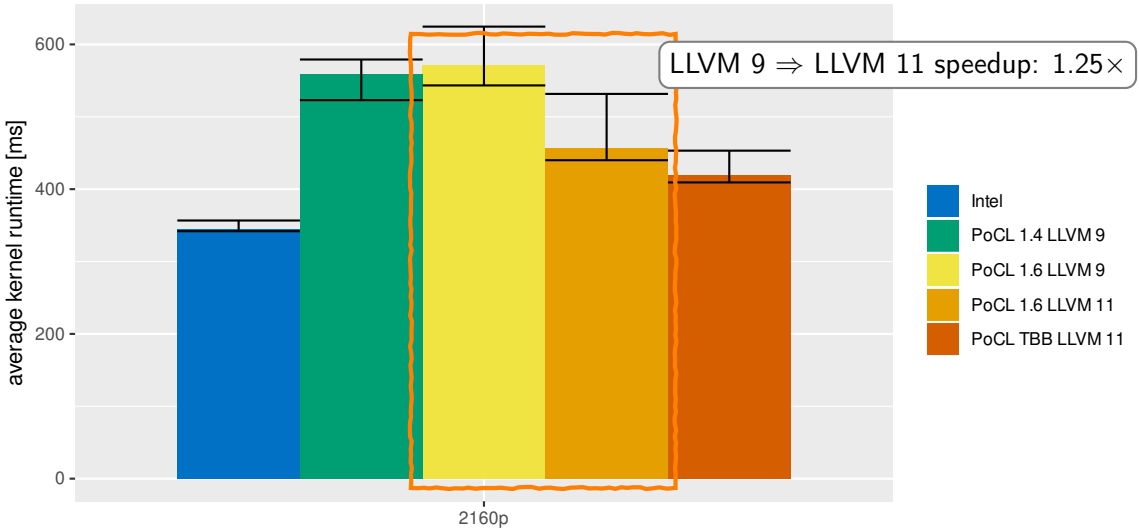

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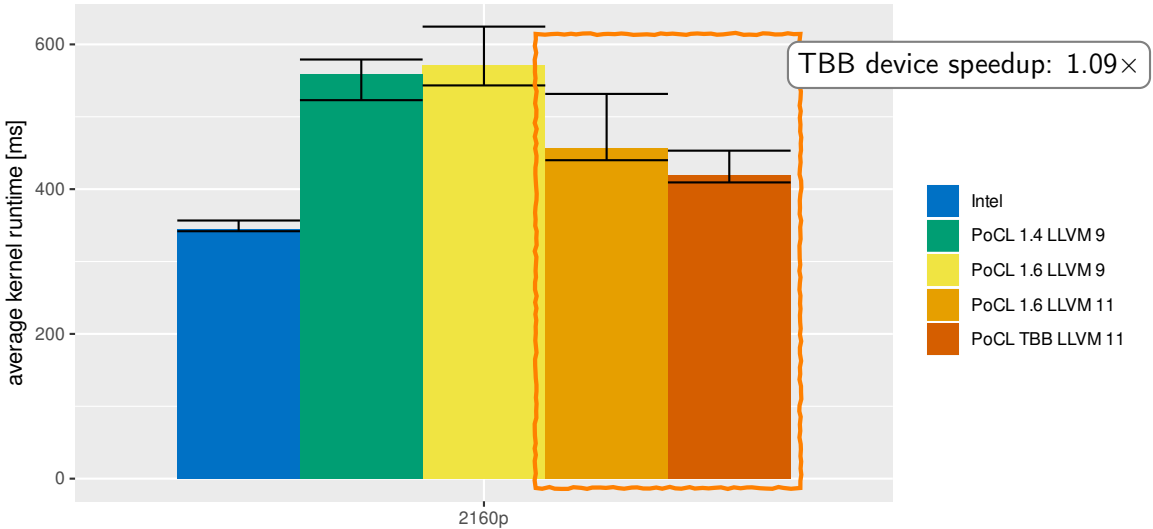

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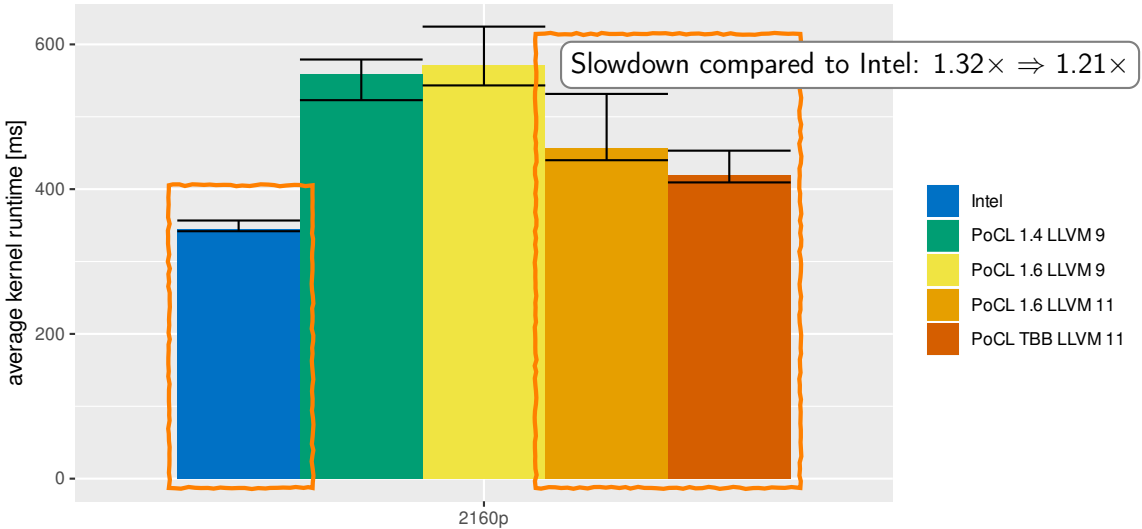

Vectorisation in PoCL

manual vectorisation

automatic vectorisation

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vfmadd231**sd** %xmm0,%xmm1,%xmm0

⇒ **no vectorisation** across work-items

⇒ inner loop not vectorisable (reduction)

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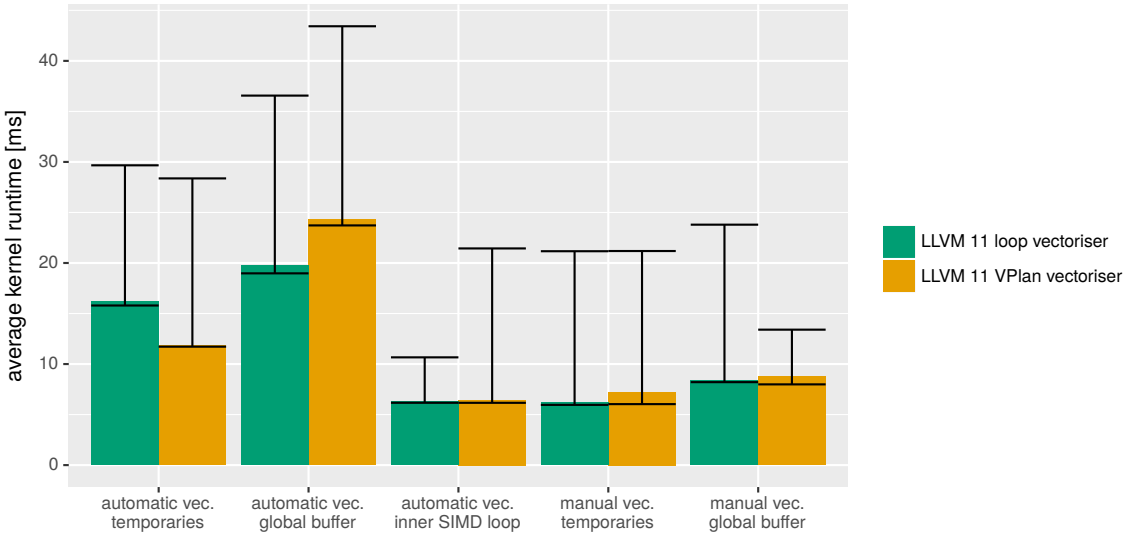
Can LLVM 11 do this?

hexciton_benchmark: LLVM Vectoriser Comparison



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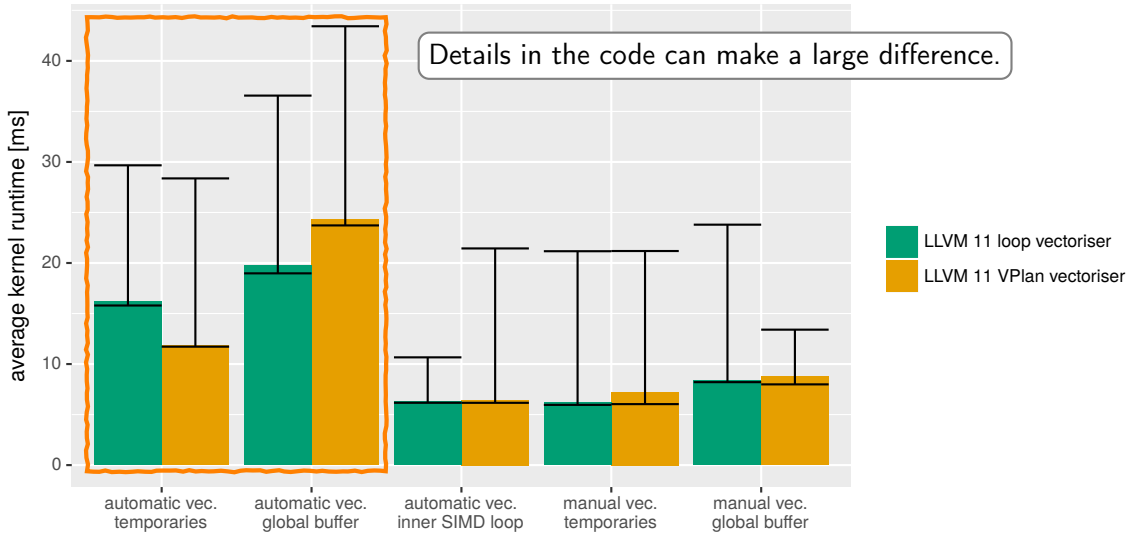

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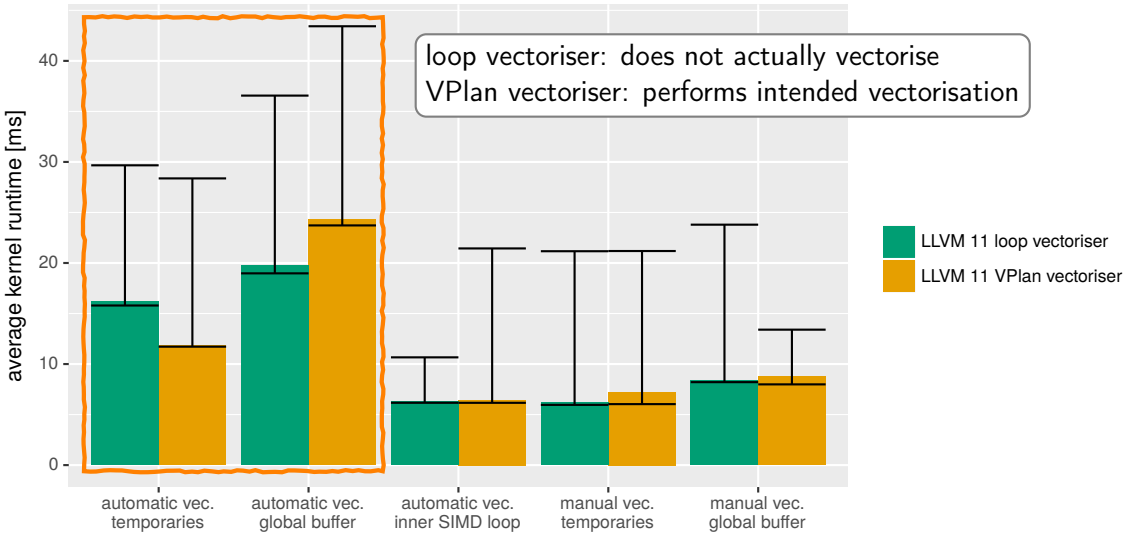

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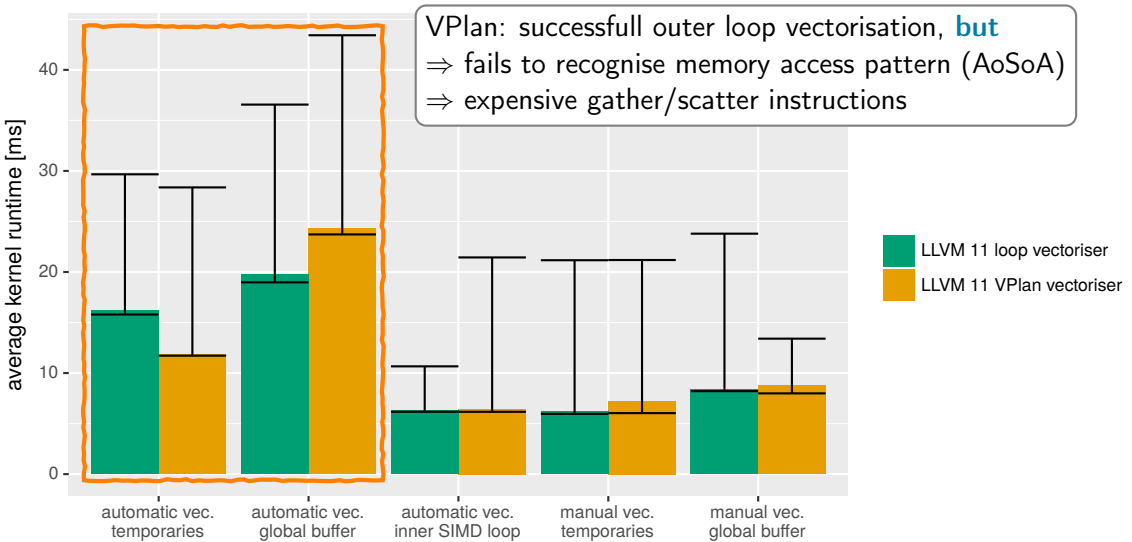

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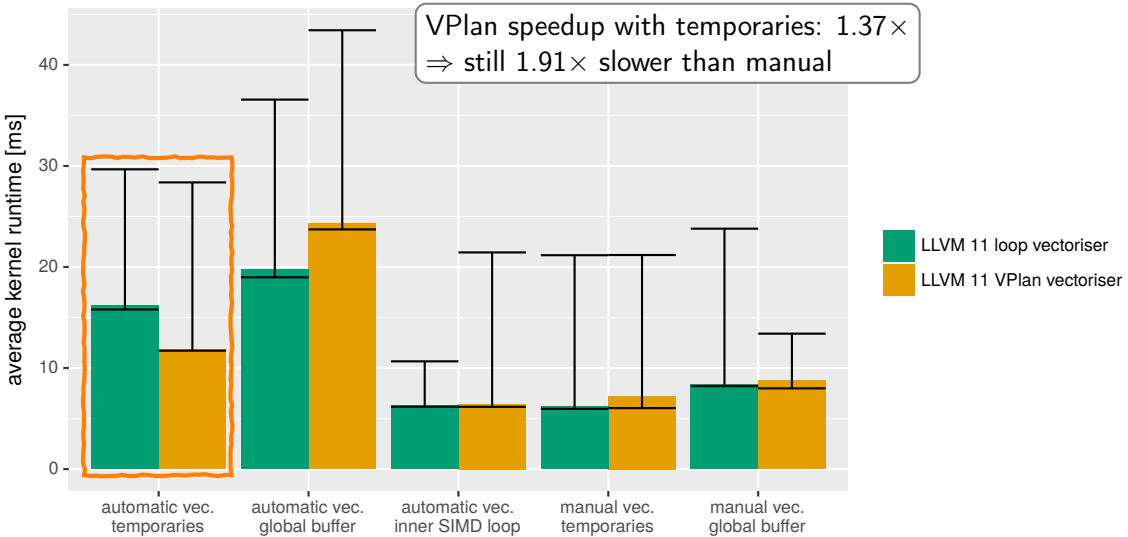

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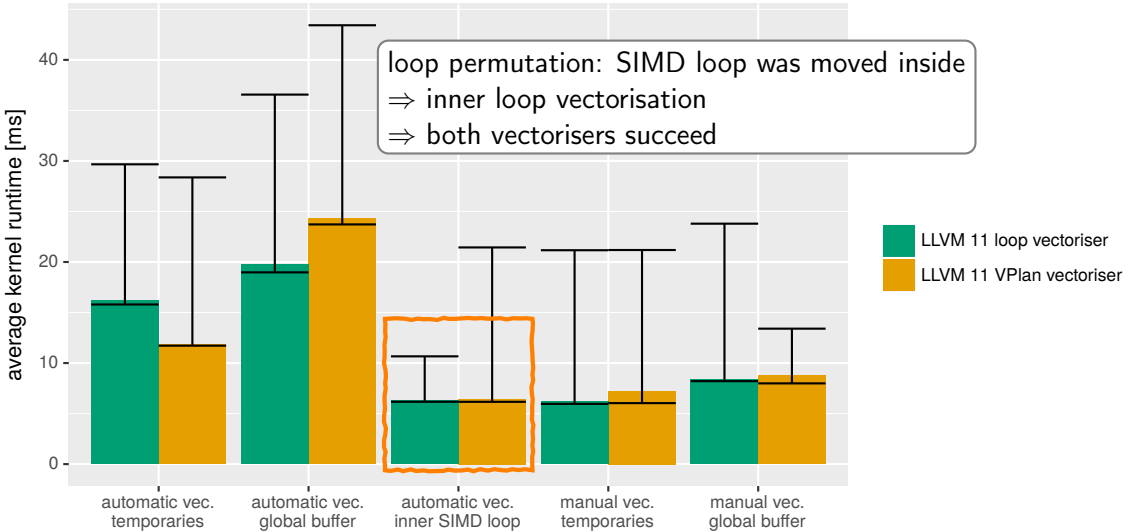

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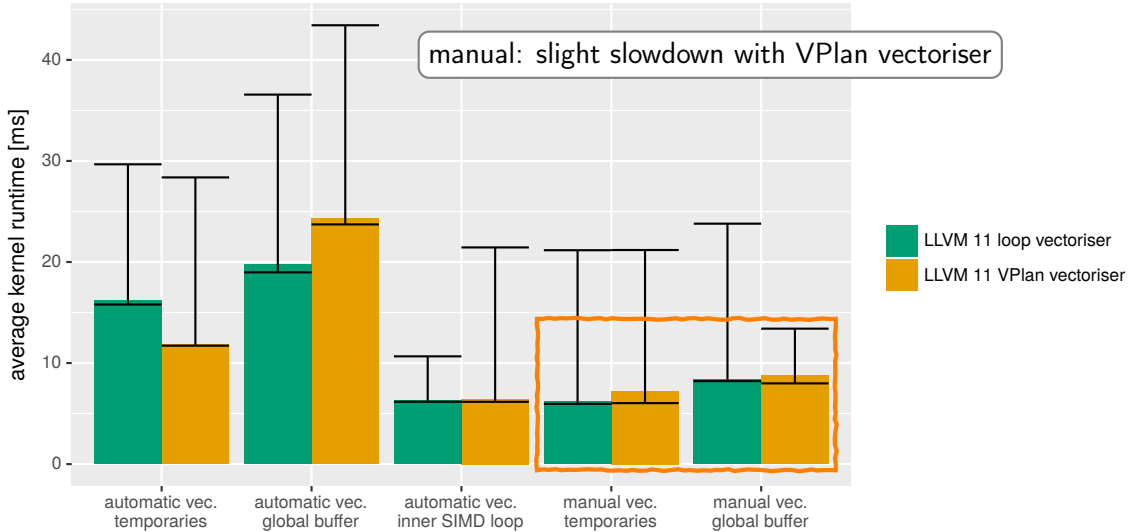

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Thank you for your attention!

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